

Reliability & Test Handbook

Phone: 408-774-9060

800-759-3735

Fax: 408-774-2169

Website:

Email: Rel@plxtech.com

Revision: Original

October 2000

© 2000 PLX Technology, Inc. All rights reserved. PLX Technology, Inc. retains the right to make changes to this product at any time, without notice. Products may have minor variations to this publication. PLX assumes no liability whatsoever, including infringement of any patent or copyright, for sale and use of PLX products. PLX Technology and the PLX logo are registered trademarks of PLX Technology, Inc. Other brands and names are the property of their respective owners.

Document Number: GEN-GEN-RH-P1

Printed in the USA, October 2000

Contents

1. Introduction	1-1
1.1 About this Handbook.....	1-1
1.2 General Information about Reliability Programs	1-1
1.3 General Information about Test Programs.....	1-2
2. Reliability Monitoring	2-1
2.1 Lead Scan.....	2-1
2.2 Packing/Shipping Monitor	2-1
2.3 Electrical Test	2-1
2.4 Characterization.....	2-2
3. Environmental Testing	3-1
3.1 Burn-in	3-1
3.2 High Temperature Operating Life (HTOL).....	3-1
3.3 Temperature Cycle	3-2
3.4 Autoclave	3-2
3.5 85°C/85% (Relative Humidity/Temperature).....	3-3
3.6 Highly Accelerated Stress Test (HAST).....	3-3
3.7 High Temperature Storage	3-4
3.8 Moisture Induced Stress Testing.....	3-4
3.9 Salt Atmosphere	3-6
3.10 Acceleration Stress Factors	3-6
4. Mechanical Testing	4-1
4.1 Lead Integrity	4-1
4.2 Bond Strength (Destructive Bond Pull Test)	4-1
4.3 Die Shear Strength	4-2
4.4 Solderability Testing.....	4-3
4.5 General Information on Solder and Solder Reflow Methods	4-3
5. Electrical Testing.....	5-1
5.1 Latch-Up Testing.....	5-1
5.2 Electrostatic Discharge Testing	5-1
5.3 Production Testing.....	5-3
5.3.1 Contact Test	5-3
5.3.1.1 DC Continuity Test	5-3
5.3.1.2 Functional Continuity Test	5-5
5.3.2 Gross I _{DD}	5-5
5.3.3 Gross Functional.....	5-5
5.3.4 Static I _{DD}	5-5
5.3.5 VIL/VIH	5-6

- 5.3.6 VOL/VOH 5-6
- 5.3.7 Leakage Test (IIL/IIH)..... 5-6
- 5.4 Device Characterization..... 5-9
 - 5.4.1 AC Parameters..... 5-10
 - 5.4.1.1 Setup Time..... 5-10
 - 5.4.1.2 Data Hold Time 5-10
 - 5.4.1.3 Output Delay Time 5-10
 - 5.4.2 Level Conditions During Characterization 5-11
 - 5.4.3 Characterization at Temperatures 5-11
 - 5.4.4 High Speed Digital Testers..... 5-11
- 6. Failure Analysis..... 6-1**
 - 6.1 Failure Mechanisms 6-1
 - 6.2 Failure Probabilities 6-1
 - 6.3 FIT Rates..... 6-2
- 7. General Product Information..... 7-1**
 - 7.1 Fabrication Process Technology 7-1
 - 7.2 Device Packaging Terminology 7-1
 - 7.3 Device Packaging Configurations..... 7-2
 - 7.4 Device Packaging Diagrams..... 7-3
 - 7.5 Part Number Definitions..... 7-4
 - 7.5.1.1 Current Part Number Labeling Method..... 7-4
 - 7.5.1.2 Former Part Number Labeling Method 7-4
 - 7.6 PLX Device Class Types 7-4
 - 7.7 Tray Types..... 7-5
- 8. References..... 8-1**
- Appendix A. Definition of TermsA-1**

Figures

Figure 1-1. Reliability Testing Structural Chart.....	1-2
Figure 2-1. Monitoring Program Flow Diagram	2-2
Figure 3-1. Temperature vs. Acceleration Factor Due to Temperature.....	3-7
Figure 3-2. Stress Voltage vs. Acceleration Factor of Voltage	3-8
Figure 4-1. Application of Applied Force in Die Shear Strength Testing	4-2
Figure 4-2. Infrared Reflow Temperature Profile.....	4-4
Figure 4-3. Vapor Phase Reflow Temperature Profile	4-5
Figure 5-1. Human Body Model, ESD Test Circuit.....	5-2
Figure 5-2 . Charge Device Model, ESD Test Circuit.....	5-2
Figure 5-3. Continuity Test Circuit for Input Pins.....	5-4
Figure 5-4. Continuity Test Circuit for Output Pins.....	5-4
Figure 5-5. Leakage Test Circuit.....	5-7
Figure 5-6. Production Test Flow	5-8
Figure 5-7. AC Timing Characteristics Diagram.....	5-10
Figure 6-1. Failure Curve for Semiconductors	6-1
Figure 7-1. PQFP Packaging, Cross Sectional	7-3
Figure 7-2. PBGA Packaging, Cross Sectional	7-3

Tables

Table 3-1. Environmental Test Parameters	3-5
Table 6-1. Calculated FIT Rate for Current PLX Products	6-2
Table 7-1. Device Process Technology	7-1
Table 7-2. Packaging Configuration.....	7-2
Table 7-3. Tray Loading	7-5

1. Introduction

1.1 About this Handbook

The *PLX Technology Reliability and Test Handbook* provides customers with an understanding of the various measures used by PLX Technology to ensure high quality product. PLX Technology has a high degree of confidence in the product that it delivers to customers. This handbook will go into some detail about various reliability practices undertaken by PLX Technology.

1.2 General Information about Reliability Programs

When manufacturing integrated circuits, reliability refers to the probability that a circuit will satisfactorily perform its intended function, under specific operating conditions, for a given time period. It is the responsibility of PLX Technology's Quality/Reliability Engineering Department to calculate and measure the probability of a product's successful operation. PLX reliability engineers simulate environmental conditions, as well as develop testing methods that accelerate the aging process of a circuit. The simulation and testing methods calculate reasonable results for the lifetime behavior analysis of a device. The collection of statistical data from the various tests plays an important role in providing a solid foundation for failure analysis. It is this data that provides the basis for improvements (if needed) to any or all currently implemented processes that impact high quality product.

There are several types of testing methods to analyze the integrity of the product. The scope of our reliability program extends from the external structure of a device to the internal circuitry. Areas such as the quality of encapsulate packaging to lead frames, internal bond wire interfaces, and metal-line electromigration are just some of the items monitored. The reliability tests are designed to examine the quality of the fabrication and assembly processes of our ASIC products.

A reliability program can be roughly partitioned into three testing phases: Mechanical, Environmental and Electrical. Mechanical testing involves testing the mechanical integrity of a product's packaging, including wire bond attachments, termination integrity and solderability, just to name a few. Environmental testing places devices under stressful conditions that accelerate the so-called "life" of a device in order to provide reasonable data to calculate failure rates and other important reliability characteristics. Finally, electrical testing is used to verify a product in its intended-operating environment. Testing programs are developed as a way of characterizing all of the DC specifications, and timing characteristics that a device must operate under. Figure 1-1 shows the various tests used in our reliability program.

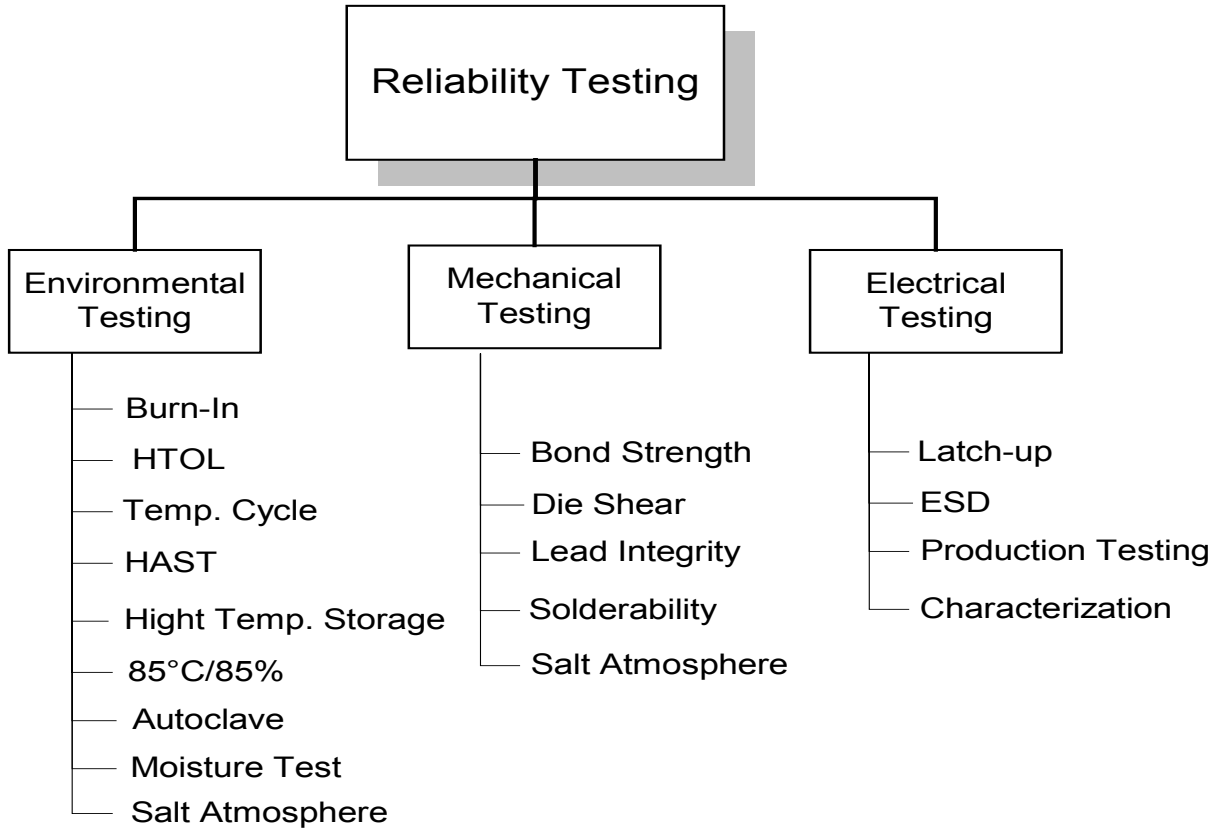


Figure 1-1. Reliability Testing Structural Chart

1.3 General Information about Test Programs

Testing is defined as the procedure in which the performance of a product is measured under various conditions. At PLX Technology, it is the responsibility of the Test Engineering Department to develop production run test programs and characterization programs that effectively test a device at either normal operating conditions, or worst-case operating conditions. The measured results of these tests can then be analyzed to verify the stability and quality of the fabrication process.

2. Reliability Monitoring

PLX Technology has implemented an internal monitoring program to monitor the finished product, shipped to PLX from its subcontractors. A system has been put in place designed to monitor the quality and reliability of the incoming product. The monitors are described in detail below.

2.1 Lead Scan

PLX Technology performs lead scan testing on a monthly basis for the purpose of monitoring the quality of package leads. Packaging leads are scanned with laser scanning machines to determine if all pin dimension measurements conform to the purposed packaging specification. Those that do not pass the laser scan test are documented and sent for reconditioning (pin correction). After a device has been reconditioned, that device is re-tested. All documentation in relation to the lead scan test is kept on file and closely monitored. In addition to the routing cards provided by the lead scan service vendor, a data log is kept containing relevant information from each months' monitor.

2.2 Packing/Shipping Monitor

Internal monitoring is performed, on a bi-monthly basis to verify that the shipping and packaging procedures are being followed in accordance to the established internal specification. Randomly chosen packages are opened inside a properly controlled environment. Visual inspections are performed noting items such as pin damage, device placement on the trays, uniform device orientation, and accurate shipping count. In addition to internal device inspections, external labeling and packaging conformance is monitored. Any discrepancies found are noted and recorded into an inspection log. The Quality Engineering and Operations departments are notified of all discrepancies. After the inspections have been completed, proper actions can be taken to correct the noted discrepancies.

2.3 Electrical Test

Electrical testing is performed on a fixed sample size each month. This test is performed with the purpose of monitoring the conformance of production product to set electrical and functional parameters. The sample size chosen for the test is reflective of the most common individually packaged bundle size for our parts in stock. All parts used for this test are from Finished Goods Inventory (FGI). This gives PLX some reference in determining the quality of the parts that are being shipped to our customers. Industry standard Automated Test Equipment (ATE) testers are used to run production test programs on the sampled devices. Numerous device parameters such as current leakage, functional performance, VOL/VOH, are measured to verify the overall performance of each device. The devices tested in the monthly monitoring program are tested at room temperature. Those devices that pass the electrical testing are placed back into stock while those that do not pass are scrapped. All test results are kept on file in addition to a data log that is used for recording important information about the test. Subcontractors are notified of any failures.

2.4 Characterization

Device characterization is performed to a specified number of devices on a quarterly basis. Periodic characterization can be used as a method of verifying the stability and quality of the device fabrication process, assembly process, and other process controls. Figure 2-1, below, illustrates the monitoring program flow.

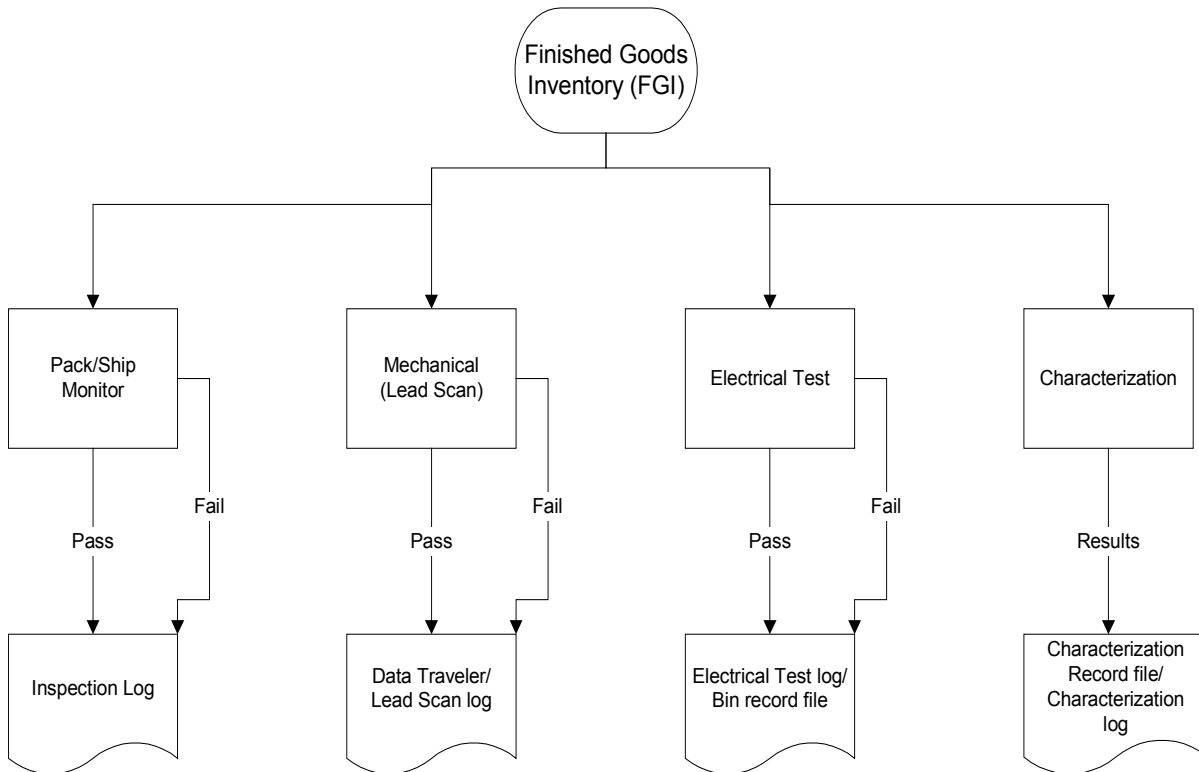


Figure 2-1. Monitoring Program Flow Diagram

3. Environmental Testing

3.1 Burn-in

Burn-in testing is performed as a way of screening out marginal devices. During the manufacturing process, a certain number of devices will be built with defects or other shortcomings. Burn-in testing is useful in screening out “infant mortality” failures. These failures occur in the early stages of a products lifetime due to manufacturing defects. Burn-in testing places devices in high stress environment. The stress conditions that are applied to devices during burn-in are an effective method of aging the devices. In particular, burn-in testing is used to check for internal metal migration or metal expansion that can effect device operation.

Devices are placed in burn-in boards. Burn-in boards are built from high temperature tolerant material that can withstand constant temperature exposures of up to 150°C. The boards are then placed into the burn-in chambers. A voltage bias higher than the nominal voltage level is applied to the devices in order to add additional stress during this test. The test is performed at 125°C for 168 hours. The burn-in method used by PLX Technology is referred to as dynamic burn-in. In this method we use numerous driver/receiver boards to generate vector patterns. The vectors generated are dynamic data stream patterns that keep signals switching high and low so that the maximum number of internal nodes will be exercised. Devices are electrically tested prior to entering the burn-in ovens, and are also tested while the burn-in process is taking place. Once burn-in is complete, devices are submitted to production testing to verify functionality. PLX Technology believes that all three levels of testing are necessary in order to provide an accurate assessment of test failures.

Failure mechanisms as a result of the burn-in test are contamination, oxidation defects, metal line electromigration, refresh degradation and silicon defects.

3.2 High Temperature Operating Life (HTOL)

PLX Technology performs HTOL testing to monitor the effects of bias conditions and high temperatures on solid-state devices over an extended period of time.

High Temperature Operating Life testing is conducted at 125°C with an applied voltage bias higher than the nominal voltage level. The test duration is for 1000 hours. Test parameters, such as time and/or temperature, can be altered in order to accelerate the test. Intermediate measurements, using the standard production test program, are made to the devices at 24, 168, and 500 hours into the test.

Failures generated are monitored and analyzed for long-term stress effects that the products are expected to undergo. Metal electromigration, oxidation, and other common high temperature and voltage stress related failures are noted as test failures.

3.3 Temperature Cycle

Temperature cycle testing is used as a method of determining the device's resistance to high and low temperature extremes. This test exposes the device packaging to mechanical fatigue induced by thermal expansion. PLX Technology uses the conditions of this test to stress the attachments between bonding pads and die surface, as well as the interface between the die and surrounding solder attachment to the package. The test results are used for reliability analysis of the assembly process.

Before devices are subjected to temperature cycle testing, electrical testing is performed to check for any noticeable electrical problems. The temperature cycle test involves the placement of a device such that the resistance to airflow is minimal. Devices are cycled for specified periods of time ($T_{cyc} \geq 10$ minutes) between high temperatures of $+150^{\circ}\text{C}$ ($+15^{\circ}\text{C}/-0^{\circ}\text{C}$), and low temperatures of -65°C ($+0^{\circ}\text{C}/-10^{\circ}\text{C}$). PLX typically runs 2-to-3 cycles per hour during temperature cycle testing. The temperature ranges used during the test are in accordance with MIL-STD-883. The test is performed for 500 cycles within those specified temperature conditions. Once the 500 cycles are completed, the devices undergo another electrical test within 48 hours, using the standard production test program for that device.

Failure criteria consist of any physical defects to the die, packaging, leads, or marking, provided damage was caused as a result of the test itself. Post electrical testing is performed at the conclusion of the Temperature Cycle Test.

3.4 Autoclave

The Autoclave test (also referred to as Pressure Pot) is performed to simulate high-pressure environments. These high-pressure environments are used to determine whether or not a device can withstand high amounts of thrust.

The test is conducted at 121°C , 100% Relative Humidity (RH) and 2 atm (atmospheres) of pressure. Devices subjected to this test are left in the chambers for 500 hours. Standard production electrical testing is performed on the devices once the 500 hours have been completed.

Potential failures resulting from the test might include device packaging implosion or explosion. Any other physical defects resulting from this test are considered to be test failures.

3.5 85°C/85% (Relative Humidity/Temperature)

The 85°C/85% test is a method of simulating potential storage conditions for a device. This test is performed for the purpose of evaluating the reliability of a non-hermetic packaged device in a humid environment and an elevated temperature.

The main aspect of this test is to place biased microcircuits in an environment of 85°C at 85% relative humidity for a period of 1000 hours. A voltage is applied to accelerate the stress levels.

After the 1000 hours, devices are electrically tested to verify functionality. Devices that cannot demonstrate full functionality via electrical testing are considered to be test failures. Any other mechanical failures or physical defects resulting from this test shall also be considered test failures.

3.6 Highly Accelerated Stress Test (HAST)

HAST is performed for the purpose of evaluating the reliability of a non-hermetic packaged solid-state device in humid environments. The extreme conditions used in this test accelerate the penetration of external moisture through the encapsulate packaging itself, or through the interface of the leads and the encapsulate package. Once the equilibrium is reached within 24 hrs of the test, the results are equivalent to 1000 hrs of 85°C/85% testing. This equivalency is due to the added stress provided by the increase in temperature.

HAST chambers must be preconditioned to specific humidity and temperature conditions for a specified duration of time. This preconditioning must be completed prior to placing HAST boards into the test chambers. The HAST testing is performed at 130°C and 85% relative humidity with a voltage bias applied to the devices. The bias is typically higher than the normal operating level as to provide a high amount of stress to those devices. Devices are placed into the HAST chambers for 200 hours. After the test is completed, the HAST boards are removed from the heating chambers and are allowed to air dry for a 1/2 hour minimum, up to a 8 hour maximum.

At the conclusion of the test, the devices are electrically tested to verify continued functionality. Devices that cannot pass electrical testing are also considered to be failures. Additionally, parts containing corrosion or cracking are also considered to be failures.

3.7 High Temperature Storage

High Temperature Storage is performed to evaluate the effects of high temperature storage conditions with no electrical stress applied to the devices. This test is used to simulate potential storage conditions for devices.

The test is accomplished by placing previously tested devices into a temperature chamber, heating the chamber to a temperature of 150°C with an uninterrupted exposure time of 1000 hours.

After the 1000 hrs, the devices are electrically tested to verify continued functionality. If a device does not pass, it is considered a failure. Other failure criteria shall include mechanical damage such as packaging cracks.

3.8 Moisture Induced Stress Testing

This test is performed to determine the moisture level classification of plastic surface mount devices (SMD) so that they can be properly packaged, stored, and handled in order to avoid various types of mechanical damage. Mechanical damage can be incurred during the assembly and/or solder reflow attachment process. This test can be used to determine the moisture class level of a device. Plastic SMD encapsulates are made of moisture permeable materials. Moisture that is inside the packaging turns into steam and expands, when devices are exposed to high temperature during vapor phase reflow or infrared reflow processes. Moisture expansion can cause internal delamination of the plastic from the chip, leadframe, or numerous other mechanical defects internal to the packaging. It is therefore necessary to determine and classify a device's moisture sensitivity level. Moisture classification is an indication of two important package characteristics. First, it indicates how long a device can be exposed to moisture before the device needs to be baked. Secondly, it classifies the amount of baking time needed to bring a device back to its original state (dry) once that device has reached moisture saturation.

Moisture sensitivity testing is performed by first performing a standard electrical test; therefore, verifying that all devices are fully functional. After functionality has been verified, visual and acoustic microscope inspections are performed to establish delamination criteria. The devices are then baked to remove all moisture from the devices so that they are considered to be "dry". Devices are then placed in temperature/humidity chambers according to specific soak requirements (level 3 devices are 30°C/60% RH for 192 hours). Once the devices have been removed from the chambers, they are allowed to air dry for a specified amount of time ($t_{dry} < 4$ hours). After the specified dry time, devices are submitted to 3 cycles of either vapor phase reflow or IR reflow. The reflow cycles have specific requirements on ramp-up and ramp-down heating rates, and maximum temperatures. After the reflow process, devices are again inspected under a microscope for external cracking. Electrical testing is once again performed to verify continued device functionality. The test requirements used by PLX Technology are based on moisture class 3 levels.

Further analysis is performed on the weight gain and weight loss of a device. Devices are weighed before and after moisture testing. Any gain in weight is due to moisture absorption. Analysis of this weight gain can be used to determine the floor life of a device. The floor life refers to the amount of time a device can be removed from dry pack until sufficient amounts of moisture are absorbed to place the device at risk during the reflow process. The weight loss or desorption of moisture can provide useful information about the baking time needed to remove moisture from a device.

Failure criteria for the moisture test include external and/or internal cracks, or room temperature electrical test failures. External cracking might include cracks to the packaging, while internal cracking can occur at bond wire/bond ball intersections, as well as the leads, die, or cracks from any internal feature to the outside of the package.

A general summary of all environmental test parameters is represented below in Table 3-1.

Table 3-1. Environmental Test Parameters

Stress Test	Method	Condition	Duration
Burn-in	MIL-STD-883, 1015	125°C, voltage bias, Dynamic data patterns	168 hours
HTOL	MIL-STD-883, 2003	125°C, voltage bias	1000 hours
Temperature Cycle	MIL-STD-883, 1010.7	From -65 to +150°C 2 - 3 cycles/hour	500 cycles
Autoclave (Pressure Pot)	JESD22-A102-B Condition D	121°C, 100% RH, 2 atm	500 hours
85°C/85 %	JESD-A101-A MIL-STD-883, 1003	85°C, 85% RH voltage bias	1000 hours
HAST	JESD-A110-B	130°C, 85% RH voltage bias	200 hours
High Temperature Storage	JESD-A103-A	150°C, no voltage bias	1000 hours
Moisture Induced Stress Test	JEDEC J-STD-020A	Class 3, 30°C/60% RH	192 hours
Salt Atmosphere	MIL-STD-883, 1009	Condition A, 35°C	24 hours

3.9 Salt Atmosphere

PLX Technology performs a Salt Atmosphere test as an accelerated corrosion test. This test is useful in determining the affects of seacoast atmospheric conditions on device packaging.

A salt solution composed of de-ionized water and sodium chloride, with a pH between 6.5-7.2, is used to provide a salt fog. A special mounting fixture is used to hold devices such that no contact is made between adjacent devices and, that devices do not shield each other from the fog exposure. The devices are placed into a temperature chamber in which the devices are submitted to 24 hours of salt fog and a temperature of 35°C. The salt fog concentration and velocity of passage are controlled test parameters, as specified in MIL-STD 883, Method 1009, Condition A.

Inspections are performed using 10x and 20x magnification at the conclusion of the test. Failure criteria for Salt Atmosphere testing includes corrosion defects not to exceed 5 percent of the total surface area, flaking or blistering. Additionally, any blurs, fading or missing mark is also inspected.

3.10 Acceleration Stress Factors

Environmental testing makes use of high temperatures and high voltage biases as a method of stressing devices. The testing temperature and applied voltage have a defined relation with the amount of stress added to a device. Both of the accelerating stress factors can cause the degrading of a device. The burn-in temperatures' relation to the amount of stress accrued by a device is given by the following relationship: (NOTE: A_T – Acceleration factor due to the applied temperature)

$$A_T(T) = e^{(E_a/k)(1/T_0 - 1/T_s)}$$

- k = Boltzmann's constant (8.617×10^{-5} eV/K)
- E_a = Activation Energy (eV)
- T_0 = normal operation temperature (Kelvin)
- T_s = stress temperature (Kelvin)

This relationship, taken from Arrhenius' equation, describes the acceleration effects due to high stress temperature ranges. This relationship is represented in Figure 3-1, as a plot of temperature vs. the acceleration factor for temperature for different levels of activation energies. Temperature stress may accelerate contamination defects and metal electromigration.

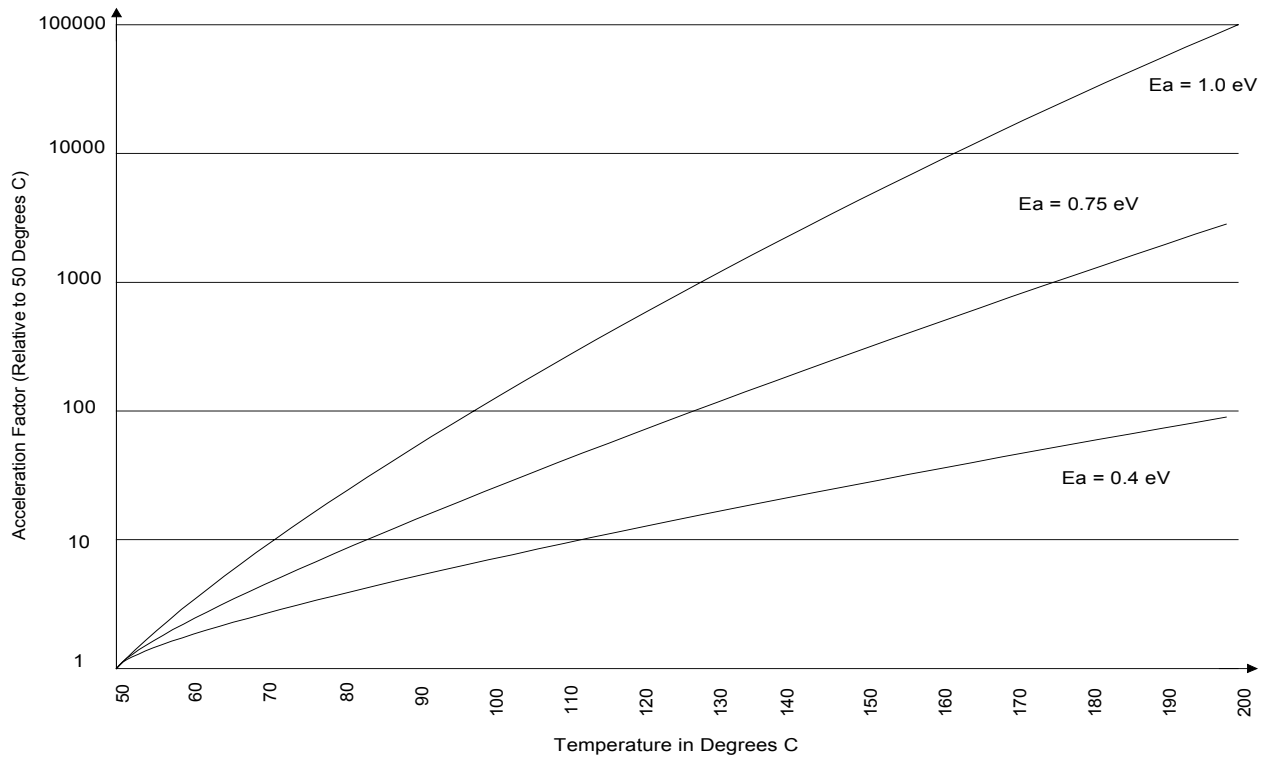


Figure 3-1. Temperature vs. Acceleration Factor Due to Temperature

The applied voltage used to stress a device is related to the acceleration factor by the relationship: (NOTE: A_V – Acceleration factor due to the applied voltage)

$$A_V(V) = e^{\beta(V_s - V_0)}$$

β = constant derived experimentally

V_0 = normal applied voltage level

V_s = stress level voltage

Typically, this voltage-stress relationship is commonly used in accelerating oxidation defects and insulator breakdown. Oxide defects can usually be accelerated by the electric field strength. Figure 3-2, shows the relationship of voltage and the acceleration due to voltage stress, relative to 5V, for various experimentally derived beta values.

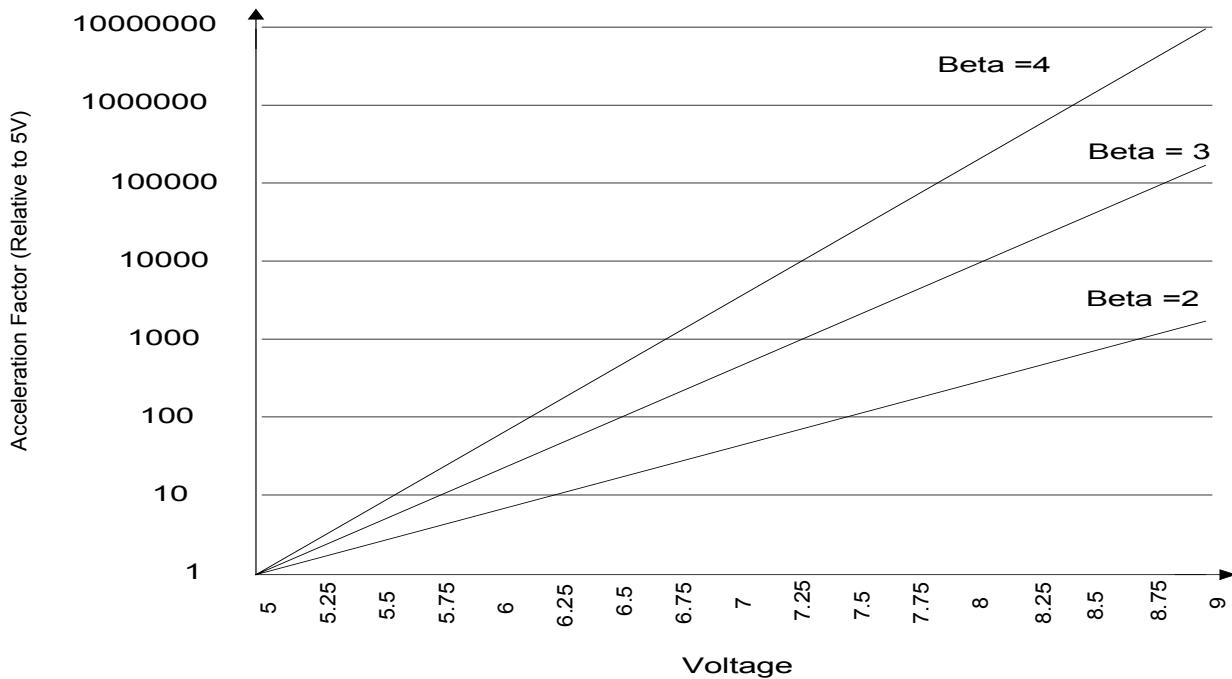


Figure 3-2. Stress Voltage vs. Acceleration Factor of Voltage

4. Mechanical Testing

4.1 Lead Integrity

Lead integrity testing is useful in determining the integrity and quality of device leads, seals, and welds. Various tests are performed based on the criteria specified in MIL-STD-883, Method 2004.5.

Lead bending is one type of testing used in determining lead integrity. Bending stress is useful in determining the capability of device leads, lead finish, and seals to withstand numerous stresses that are expected to occur in the actual handling and assembly of a device. PLX Technology requires that a specified number of random sampled PQFP devices have each individual leads bent at a 90° angle and then back to its original position. This process is repeated a second time. Once the devices have been subjected to this test, they are inspected under 10x and 20x magnification. Failure criteria for this test include breakage, cracking, loosening, and relative motion between the lead and device body.

Another type of testing used in determining lead integrity is a tension test. Tension testing is useful in determining the capability a lead has to withstand a straight pull. In this test, a force apparatus is used to pull on each lead with a force of 2.5N for a timed duration of 10 seconds. All devices are inspected under 10x magnification for failure criteria similar to those used in the bending stress test.

4.2 Bond Strength (Destructive Bond Pull Test)

Destructive bond pull testing is performed in order to determine bond strength magnitudes and distributions, as well as determine compliance with bond strength specifications. Bond pull can be applied to numerous bonding interfaces such as wire-to-die, wire-to-package lead, or wire-to-substrate bonds. The wire composition, wire diameters, and the bonding process itself are used in determining wire bond strengths.

The test condition used within PLX Technology for destructive bond strength testing is MIL-STD-883, Method 2011.7 condition D. This particular method, which is commonly referred to as wire pull, is employed on the internal bonds at the substrate and the lead frame. Stress is applied at both interfaces of the bond wire simultaneously, wire-to-die and wire-to-leadframe. This test involves the insertion of a hook on the bond wire centered between the die and the leadframe. Applying a force in a direction normal to the bond wires path stresses both interface attachments. The amount of force applied to the wire is dependent on the composition and diameter of the bond wire. Typical applied force ranges are between 1.5-15.0 gram force. The force is applied until the wire snaps or bonds lift. The criteria for failure from this test are bond lifting (failed bonds) at either interface, lifted metallization from the die or substrate, or fracture of the die or substrate.

4.3 Die Shear Strength

Testing of die shear strength is important in determining the integrity of materials and the procedures used for attaching the die to the packaging substrate. The amount of force needed to separate the die from the substrate depends on the size of the die and is specified in MIL-STD-883, Method 2019.5. A die contact tool is used to apply force to the die/substrate interface from two sides of the die. The tool is then rotated to make a 90° angle with the substrate and apply a third force to the interface. The contact tool used is approximately the same width as the die being tested. This provides for an even distribution of force along the edge of the die. Figure 4-1 demonstrates the application of applied force in die shear strength testing. Failure criteria for die shear testing are: 1) separation of die with less than 1.25 times the minimum amount of force required, and 2) evidence of less than 50% left of die attach adhesive or less than 2.0 times the minimum force with less than 10% left of die attach adhesive.

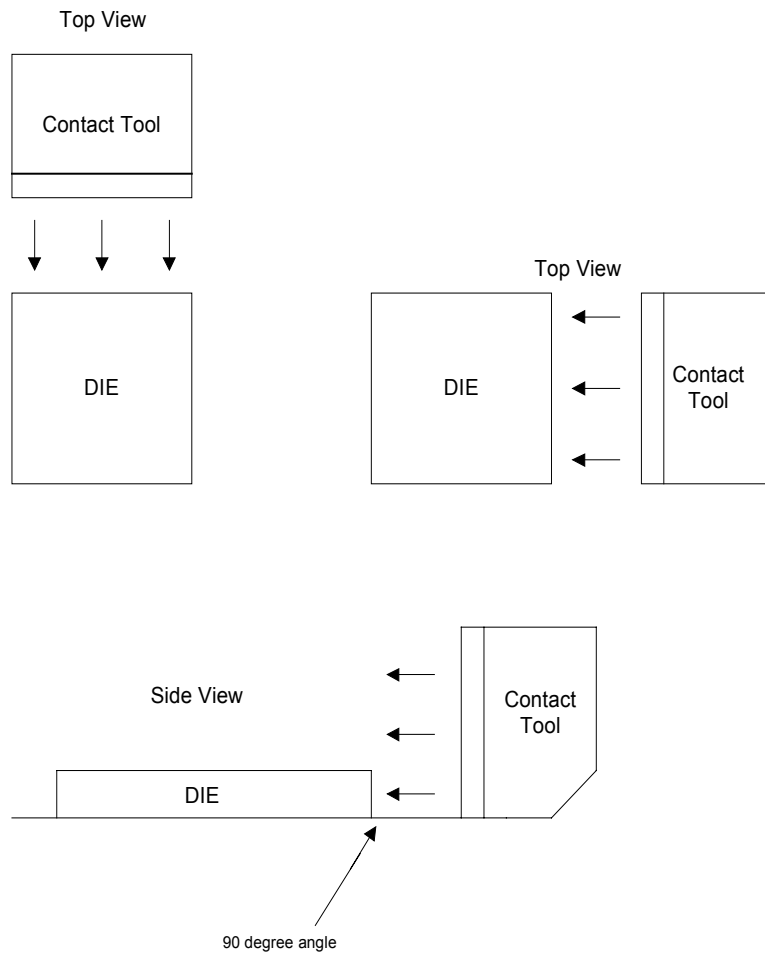


Figure 4-1. Application of Applied Force in Die Shear Strength Testing

4.4 Solderability Testing

Typically, solderability testing is performed in order to verify the solderability of device package terminations, which are intended to be joined to another surface using solder for the attachment. The test is designed to answer the question, “Will solder properly attach onto the device leads?” PLX Technology realizes that testing for solderability can be useful in identifying various problems before devices are used in the solder reflow process.

To test for solderability, the terminations of a device are held by a clamp to a force sensor. Prior to solder submersion, device terminations are dipped into a specified type of solder flux. The device is then immersed with the terminations being perpendicular with the solder, at a specified rate until the terminations are submerged. The solder should be at least 3mm away from the device package. The solder pot contains at least 2 lbs. (4.4 kg) of molten solder at 245°C. The termination is left there for 5 seconds and then emmersed from the solder pot at a specified rate. The flux will then begin to activate and clean the lead’s surface, and force pushing against the lead will then be reduced. The force reduction is recorded and measured so that the data can later be compared to the results of a known “good” device. After the test has been completed, the dipped portion of the termination is manually examined using a microscope.

There are several failure mechanisms when testing for solderability. One common failure type observed is the non-coverage of the total submersed surface area. The dipped portion of the termination should be no less than 95 percent covered with a continuous new solder coating. Some other common failure criteria are non-wetting, de-wetting, pinholes or voids. The lack of solder in certain areas is referred to as non-wetting. Non-wetting is typically due to the degradation of the composite alloy layer around device terminations. It is that surrounding alloy that provides for the attachment of solder to the lead terminations. De-wetting is the condition where molten solder has coated a surface and receded leaving irregular shaped mounds of solder. Voids or pinholes refer to imperfections that penetrate entirely through the solder layer.

4.5 General Information on Solder and Solder Reflow Methods

Reflow refers to the liquidus state of solder. When solder is in this liquidus state, it is used to attach devices onto a printed circuit board (PCB). The most common solder alloy used in electronics is a tin/lead composite referred to as Sn63Pb37. This notation refers to the alloy’s composition of 63% tin and 37% lead. This composition ratio was chosen in order to reduce the melting point of solder down to 183°C (Note: melting point of Tin (Sn) is 232°C, melting point of Lead (Pb) is 327°C). There are two popular methods used to bring solder to a liquidus state. One method is called Infrared reflow. Infrared (IR) reflow in particular refers to the heating mechanism (infrared radiation) used to bring the solder paste to a liquidus state. One advantage for using infrared radiation for reflow is that it is well controlled. A disadvantage for using this method is that when a device is in direct exposure of the light it only heats the exposed area. Any area that is shaded, such as a solder joint, does not heat as well. The other method used to bring solder to a liquidus state is vapor phase. Vapor phase heats an inactive solvent to produce vapor through which the PCB passes through for

soldering. The benefit of vapor phase reflow is that the temperature can be maintained uniformly. The risk of oxidation and contamination is minimized due to the use of the inactive solvent. The specific heating and cooling times and rates for the IR and vapor phase reflow processes are shown in Figures 4-2 and 4-3 respectively.

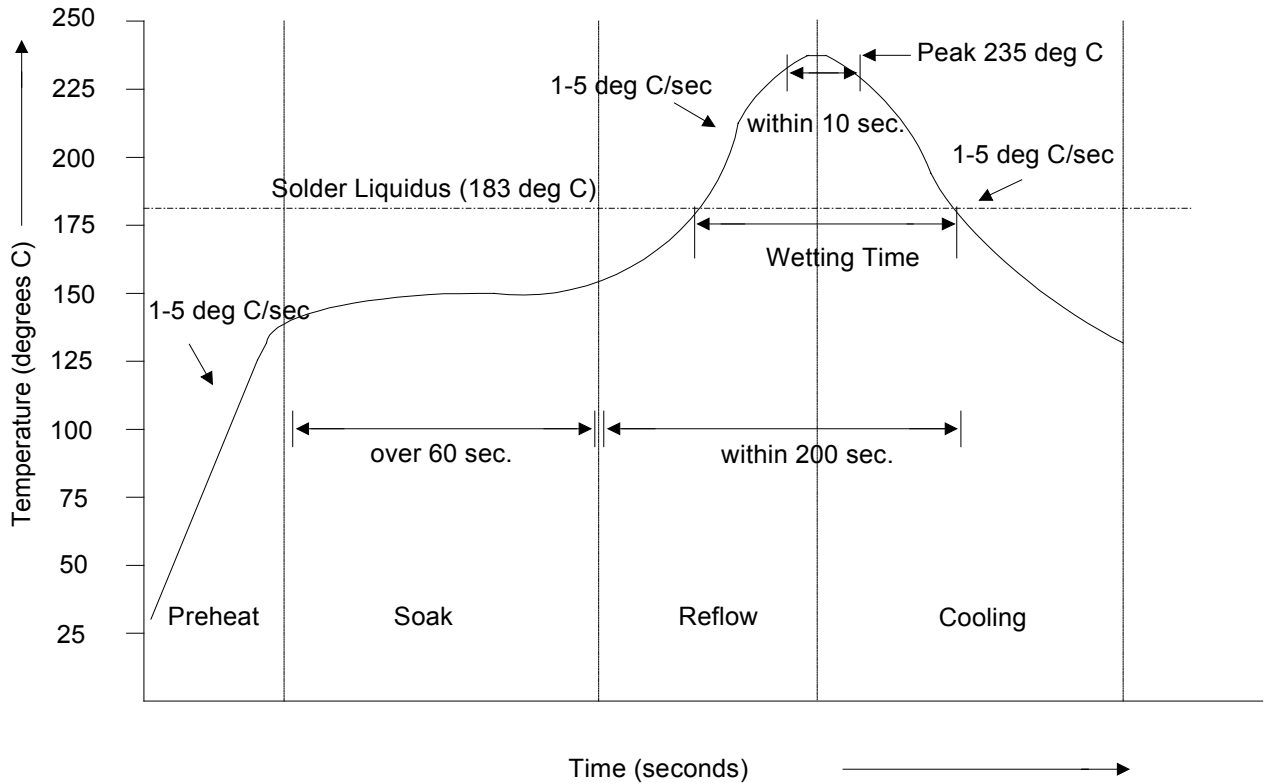


Figure 4-2. Infrared Reflow Temperature Profile

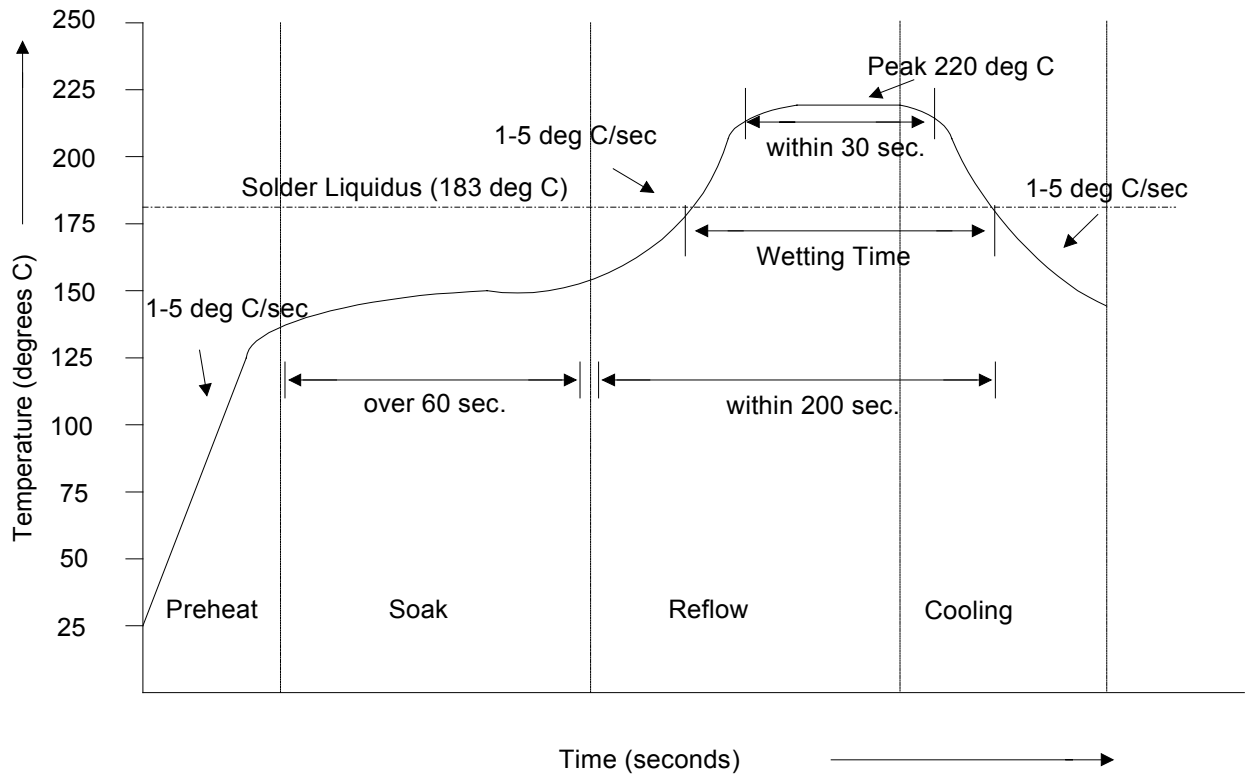


Figure 4-3. Vapor Phase Reflow Temperature Profile

5. Electrical Testing

5.1 Latch-Up Testing

Latch-Up is defined as the generation of a low impedance pathway in CMOS chips between the power and ground rails due to the interaction of parasitic PNP and NPN bipolar transistor structures sometimes triggered because of input, output, or supply overvoltages. Those interactions can essentially short the power and ground rails through a positive feedback mechanism thus causing excessive current flows, which can in turn cause damage to internal circuitry. PLX Technology performs latch-up testing in order to determine the susceptibility of our products' internal CMOS circuitry to the formation of latch-up. This test can be a particularly effective method of determining the susceptibility of latch-up as long as it can be determined that all damage caused was due to latch-up formation. For instance, if a device's quiescent power supply current is out of specification or supply voltage has "collapsed", the device should be examined electrically to determine whether the device was damaged without latch-up formation.

The basic test sequence consists of first applying a power supply voltage. One constraint is that I_{CC} (power supply current) is limited to 100mA. Next, a functional pattern is run in order to set up the input/output into a desired state. A trigger source is then applied for a specified period of time ($10\mu s < t_{trigger} < 5s$) depending on whether or not the trigger source is being applied manually or by an automated tester. After the trigger source has been applied, the supply current is measured. If $I_{CC} \geq$ test limit, the power supply should be removed so that the device can be inspected for electrical damage. To inspect for electrical damage, a device is electrically tested with particular attention placed on checking I_{DD} levels and current leakage. The magnitude of the trigger source level required to initiate latch-up is the reference used in determining susceptibility. Latch-up testing is performed at different temperature and supply voltage ranges. Worse case conditions for latch-up formation are high temperature/high voltage and the lowest value for trigger current measured.

5.2 Electrostatic Discharge Testing

Electrostatic discharge or ESD testing is performed as a method of classifying a circuit's susceptibility to damage or degradation caused by the transfer of electrostatic charge between a circuit and another body (Human Body Model or Charged Device Model) at different potentials. Electrostatic discharge is one of the most common reasons for chip failures during manufacturing and field operations. The discharge can be caused by either the contact of two bodies or by static induction. The protection networks that are built into the I/O circuitry of PLX devices are designed to filter out ESD effects before they damage internal logic circuitry.

In order to test for ESD susceptibility, various models have been designed to simulate human-circuit interactions and machine-circuit interactions. The Human Body Model, commonly referred to as HBM, is used to simulate the build up of static charge that can occur in human beings during everyday situations (i.e. walking on synthetic carpet). MIL-STD-883, Method 3015, provides the specification for testing ESD susceptibility.

PLX devices are classified to withstand static voltage stresses greater than 2 kV and are therefore classified as class 2 devices. The test, which is considered to be a destructive test, is performed at room temperature. The basic form of the test is the charging of a 100pF capacitor to a specified voltage level. Once the capacitor is charged a high voltage relay connects the charged capacitor to a circuit containing the DUT. Once the capacitor is connected to the test circuit, it discharges through a 1.5 kΩ resistor into the DUT. After the test is performed, the DUT is verified by production electrical testing. The test is repeated at increased voltage levels until a failure can be verified by electrical testing.

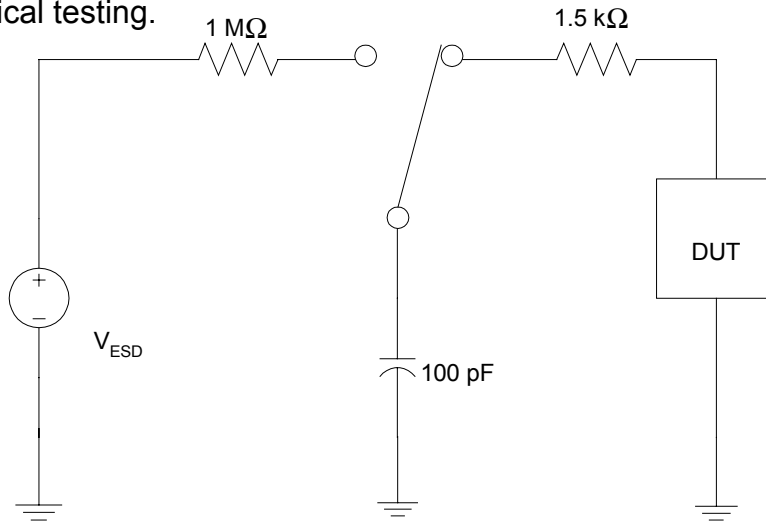


Figure 5-1. Human Body Model, ESD Test Circuit

Another ESD model that is used is the Charged Device Model. This model simulates the discharge of packaged integrated circuits. Devices can accumulate charge during the assembly process and/or the shipping process. Charged device testing involves charging a device through a $1\text{ G}\Omega$ resistor, disconnecting the charging supply and discharging the device to ground. After testing the Charged Device Model, electrical testing is performed on the devices to verify that no damage was caused due to the test. Figure 5-2 shows the schematic for Charged Device Model testing.

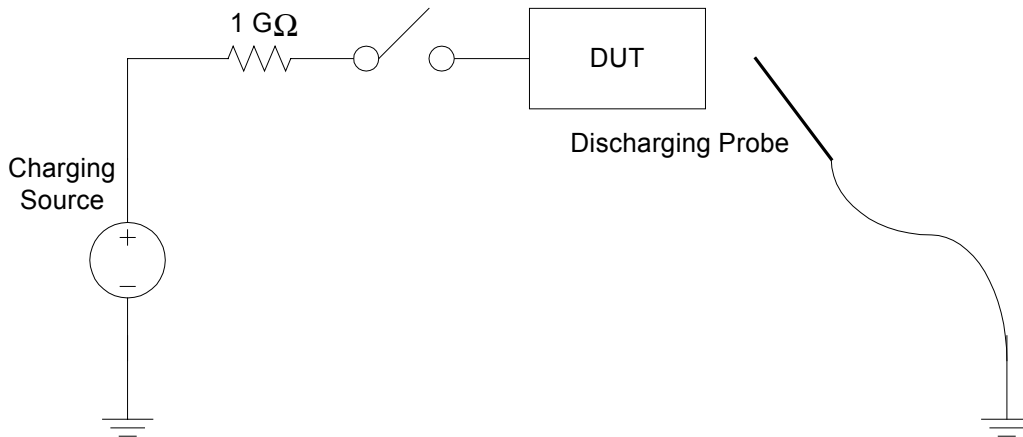


Figure 5-2 . Charge Device Model, ESD Test Circuit

5.3 Production Testing

In order to perform all of the necessary electrical testing that production parts should be subjected to, a standard production test program has been developed to verify intended device requirements and characteristics. Production testing involves testing numerous DC parameters as well as testing the functional operability of a device. The following describes in detail the various elements within the production test flow.

5.3.1 Contact Test

This test identifies whether contact is made to all of the device's signal pins, as well as checking for signal pin shorts.

5.3.1.1 DC Continuity Test

V_{DD} is not supplied to the DUT while this test is running, and all pins are tied to ground. Current is forced to each pin, one at a time using a PMU, through the protection diodes, and then the voltage drop across the diodes measured. Forcing a current of $100\mu A$ to the protection diode that is connected to V_{DD} , and $-100\mu A$ to the protection diode connected to ground will forward bias each respective diode. Once the diodes are forward biased, the voltage drops are measured and should result in $\pm 0.7V$ for each respective diode. A measured voltage drop greater than a set parameter (usually voltage $> \pm 1.2V$) would indicate an open circuit. Measured voltage drops of levels less than or equal to $0.2V$ indicate a short circuit. Figure 5-3 and Figure 5-4 depict exactly what is being tested during DC continuity testing.

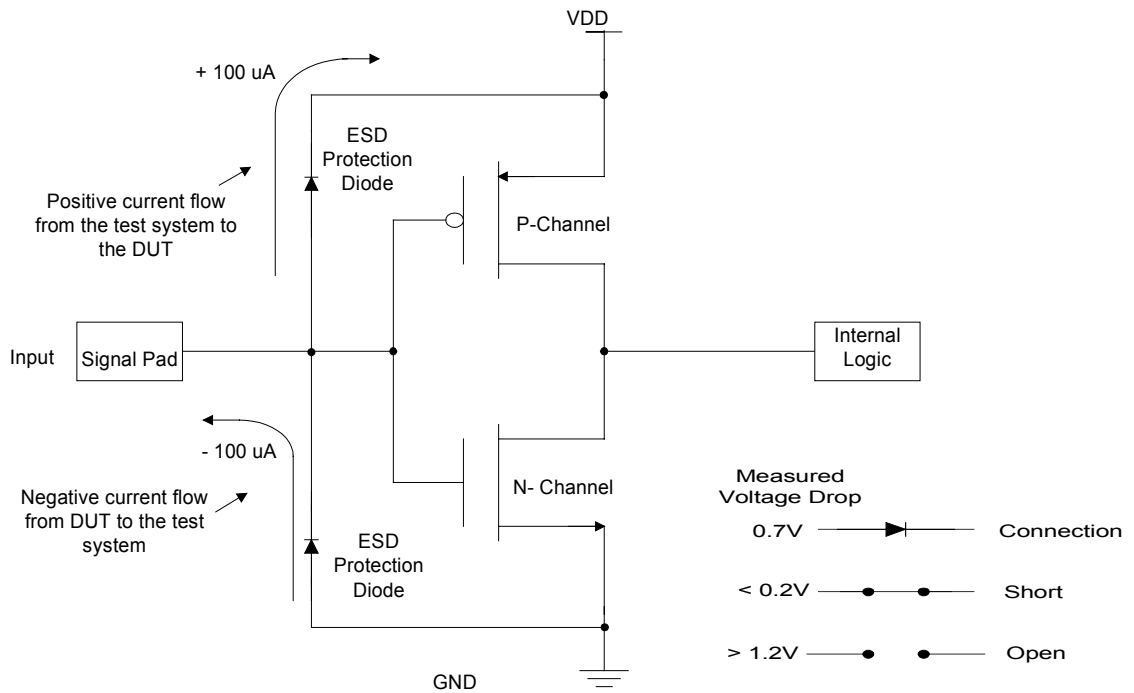


Figure 5-3. Continuity Test Circuit for Input Pins

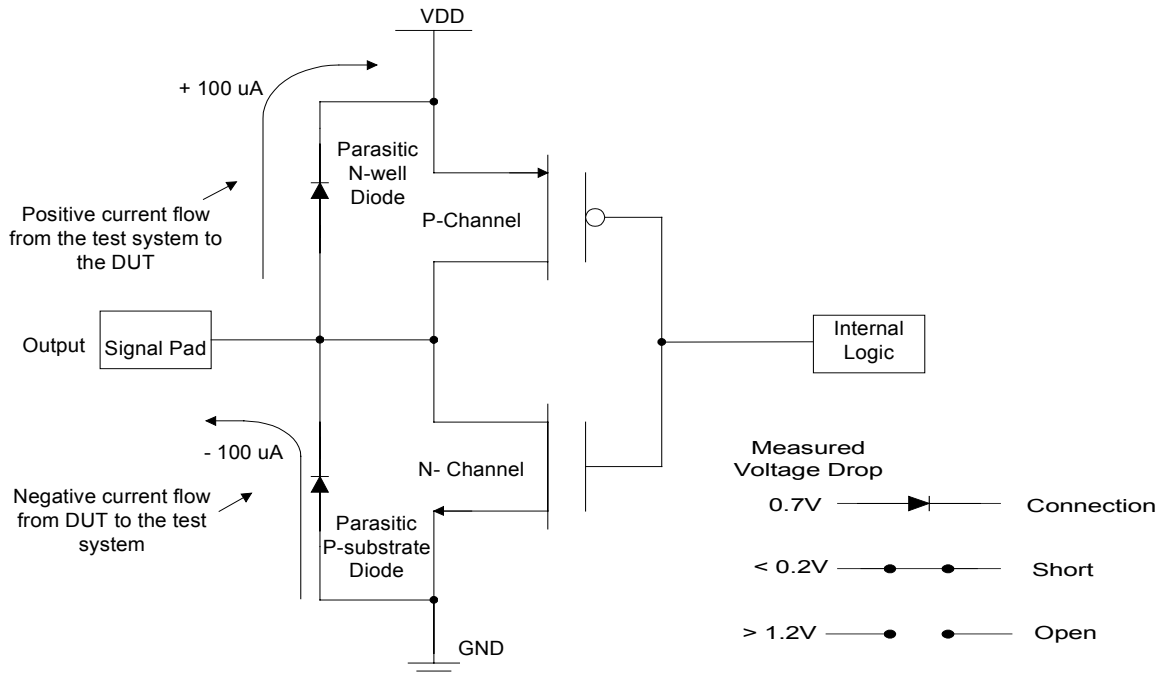


Figure 5-4. Continuity Test Circuit for Output Pins

5.3.1.2 Functional Continuity Test

This method of testing the protection diodes involves supplying the DUT with V_{DD} and running a preconditioning vector pattern. The outputs are set to a tri-state mode. The vector pattern will usually drive all of the input pins to ground, and float each pin one at a time, measuring the diode voltage at each output. If the output is measured as tri-stated, the pin will pass. If the output measures low, the pin is shorted. If the output measures high, the pin is open.

5.3.2 Gross I_{DD}

The Gross I_{DD} test is typically used to check the V_{DD} lines for unacceptably large amounts of current and determine the range of I_{DD} supply current that a device draws. V_{DD} is supplied to the DUT during this test. All inputs are set either high or low, and no switching circuits are active. The tester will then measure the current flowing through the V_{DD} lines into the device. If the amount of current is less than the specified amount (usually gross $I_{DD} < 10$ mA depending on the device), the DUT will pass.

5.3.3 Gross Functional

This test is used to verify that the DUT can accomplish all of the necessary logical functions that it is intended to perform. Gross functional testing is usually performed at lower speeds (1-10 MHz). This is done because speed is not a concern at this point in the test flow, only the device's functionality. Various test vectors are run to verify that all of the internal logic components of the DUT are working properly. Functional testing is run at three different levels of V_{DD} , which are reflective of a particular device's supply voltage level and tolerance values. During the gross functional test, all VOL/VOH/VIL/VIH margins are measured loosely. Later tests involve more restricted conditions for noise margin. To pass the gross functional test, a device must produce expected logical outputs corresponding to the input vector patterns that are run by the test system.

5.3.4 Static I_{DD}

This test is implemented to measure current leakage during static conditions after the device has had previously active switching circuits. The Static I_{DD} test is usually conducted after gross functional testing. A specific test vector is run thus preconditioning the device to a preferred state. Once in that preferred state, the vector pattern is terminated leaving the device in a static condition. This condition is considered a stand-by mode. All signals are pulled to their inactive levels. In this state, the DUT draws the least amount of I_{DD} . Once the test pattern has stopped and the device is held static for a specified amount of time, currents flowing into the V_{DD} pins are measured. If the measured current is below a specified amount the device will pass.

A sub-test that falls within this test description is that of I_{DDQ} . I_{DDQ} can be useful in testing for fabrication defects by determining exactly which area of the chip has high static current. I_{DDQ} is the measurement of the static current within a specific area of the chip. If a static current level of a specific circuit block is known, that current can be

measured and compared with the expected results. This method provides an effective way of narrowing down possible regions of erroneous operation, as well as determining any bridging faults.

5.3.5 VIL/VIH

The VIL/VIH test is a test designed to check noise margins for all of the inputs pins. The test involves a toggling of all of the output signals while sending in an input signal. If the input is correctly viewed as high or low, depending on the anticipated input, the DUT will pass. If the noise generated by the toggling of outputs interferes with the proper interpretation of the signal, then the DUT will output an incorrect response to the input, thus resulting in a test failure.

5.3.6 VOL/VOH

The purpose of the VOL/VOH test is to verify the levels that are being produced at the output pins, are within the proper ranges to interpret a signal as logic-0 or logic-1. One method of measuring VOL/VOH is a static method. In this method, to measure VOL the tester sinks a specified amount of IOL current into each of the output pins, and the PMU measures the voltage at that pin. VOL measurements for TTL Compatible CMOS devices should typically be less than 400mV. To measure the VOH, the output pin sources a specified amount of IOH current and the voltage at that pin is measured by the PMU. VOH measurements should be greater than 2.4V.

Another method of testing VOL/VOH is a functional test. This test is accomplished by re-running the test vectors used during the gross functional test, except that in this circumstance the noise margins for the outputs are set with a more restricted set of level specifications. A comparator with preset levels is used to check the output values. The test vectors used in this test should test for all outputs at both high and low levels.

5.3.7 Leakage Test (IIL/IIH)

The current leakage test is used to monitor the amount of current that leaks from the V_{DD} line to the input line and the input line to the GND line for all device input pins. The test is performed only on input pins. To measure current leakage across the p-channel transistor (IIL), the input voltage needs to be high so that the p-type transistor is turned-off. Pin drivers force all inputs high (logic-1), and then individually force each pin to GND one at a time. Once the input has been toggled low, current is measured between the input line and the V_{DD} line. This value should not be less than $-10\mu\text{A}$. To measure current leakage across the n-channel transistor (IIH), the input voltage needs to be low. This sets the n-channel transistor into a "turned-off" state. Once all of the input voltages are driven low, each input pin is toggled high individually. Current is then measured between the input and ground lines. The amount of current measured depends on numerous factors. For instance, a standard input pin like the one shown in Figure 5-5 will have leakage current in the range of $\pm 10\mu\text{A}$. An input pin with a pull-up or pull-down resistor will have a different level of leakage current than the standard input pin.

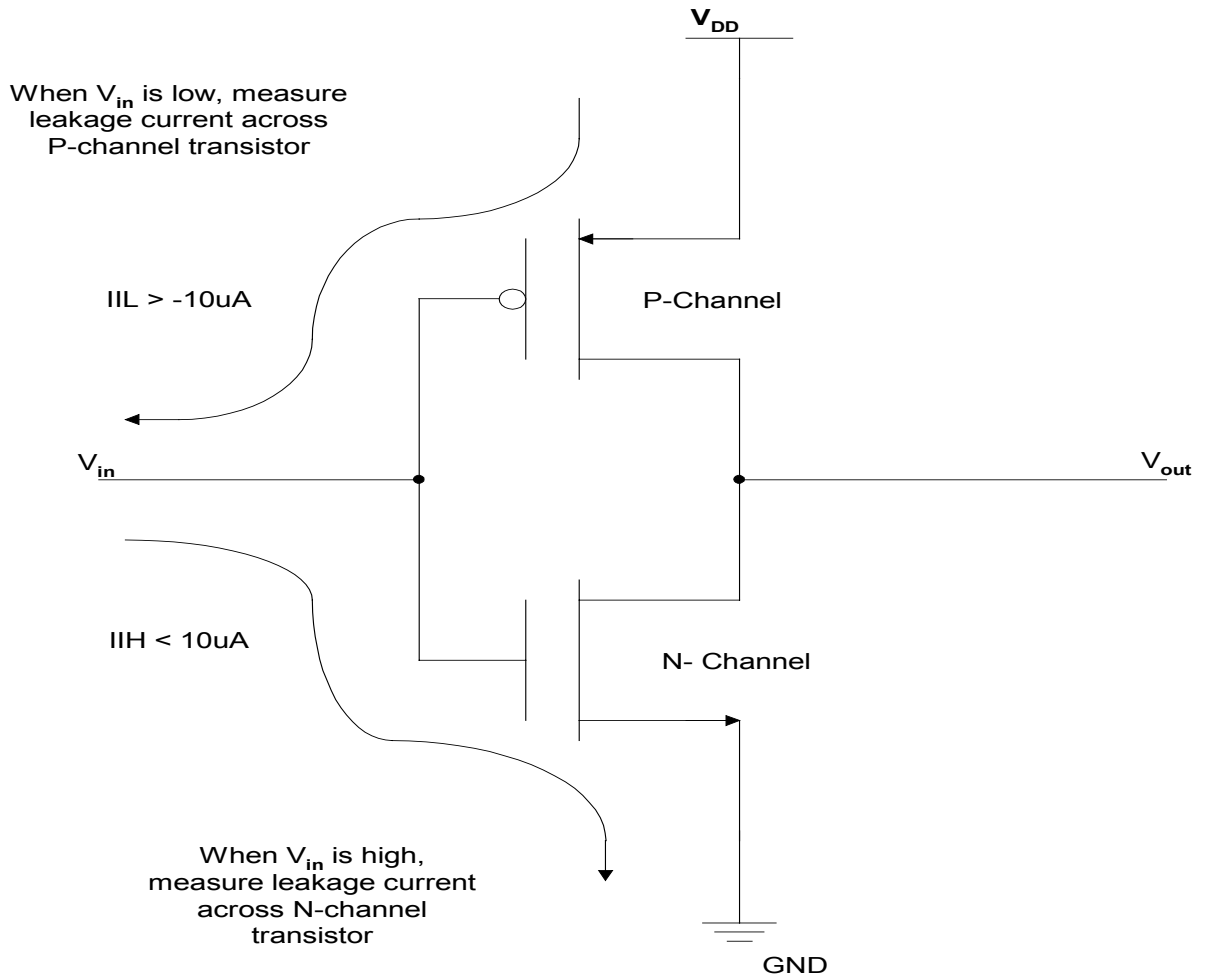


Figure 5-5. Leakage Test Circuit

The production test flow is represented in Figure 5-6.

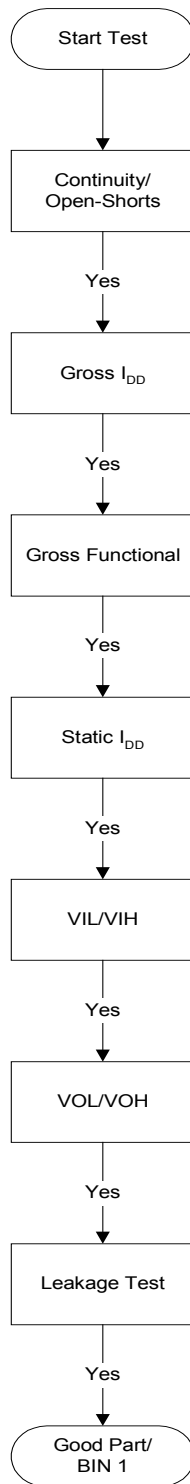


Figure 5-6. Production Test Flow

5.4 Device Characterization

What is characterization?

PLX Technology uses device characterization as a method of determining and verifying specific information about the performance characteristics of our product. Typically, high-speed CMOS designs need to be verified to make sure that strict timing requirements are met. Characterization is the validation of specified timing and level requirements for a given circuit. Once a physical piece of silicon is produced, characterization is performed to verify that a device can meet worst-case timing requirements under given level parameter constraints.

Why characterize a device?

1) *Verify the fabrication process.*

One of the main benefits of device characterization is the capability of verifying the fabrication process. The information collected during characterization can be closely monitored for significant changes. If for example drastic aspects of device timing change significantly, steps are taken to make certain that the fabrication process has not changed.

2) *Verify that a device meets design specifications.*

Characterization data is collected and compared to design specifications. Verifying input timing parameters such as set-up time and data-hold time can be useful in determining the speed of device signaling. The smallest amount of time that an input signal needs to communicate its data, the faster that signal can return to perform other tasks. A detailed description of both input timing parameters will be discussed in the following section. Characterizing the delay timing for output signals is another important aspect of device characterization. This information is useful in determining the response time of an output signal.

5.4.1 AC Parameters

There are three main AC timing parameters evaluated during characterization: setup time, data hold time and output delay. Figure 5-7 illustrates the relationship between those signals with reference to the clock signal.

5.4.1.1 Setup Time

The purpose of characterizing the set-up time of an input signal is to check that a device can meet the worst case (maximum) time a signal needs to setup before a referencing clock edge switches high or low. Setup time is defined as the amount of time a signal needs to set up into a valid state before a referenced clock reaches a certain voltage level (typically 1.5V). To prepare for testing this parameter, setup defining the appropriate timing values and signal formats as required by the timing specifications for a particular device. All functional test vectors are then run in order to exercise the necessary logical functions so that appropriate measurements of setup timing parameters can then be made.

5.4.1.2 Data Hold Time

Characterizing this parameter is useful in identifying the maximum amount of time that an input signal must hold onto its data after the referenced clock edge. Data hold time is measured when the referencing clock reaches a certain voltage level (typically 1.5V). Data hold time is verified for meeting its worst-case condition (maximum hold time). The setup of this test is similar to the setup timing parameter test. Typically, the two parameters can be tested at the same time.

5.4.1.3 Output Delay Time

Output delay timing is measured in order to identify the amount of time between the transition of one signal and the resulting transition of another signal. If the amount of delay is too large than the timing of a system can be off. Output delay is formally defined as the time it takes for an output to become valid after the triggering edge of a referenced signal (triggering clock edge). After the appropriate signal formats and timing edges have been setup, a test strobe can be programmed to check for valid levels at any time during the tester cycle.

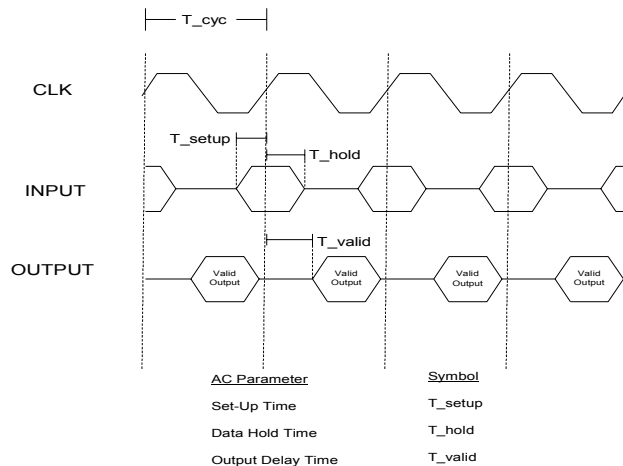


Figure 5-7. AC Timing Characteristics Diagram

5.4.2 Level Conditions During Characterization

During characterization, input voltage levels are controlled so that worst-case VIL and VIH levels may be determined. Input signals are driven with VIL set to 0V, and VIH set at V_{DD} . To determine the maximum VIL level, the tester increments VIL until incorrect output voltages are produced. Minimum VIH can be measured in a similar manner by decreasing the VIH level until incorrect outputs are produced. These settings are used to verify that signals are being properly interpreted as logic-0s or logic-1s. At the same time, outputs have their high-Z state set at 1.5V. Anything greater than 1.5V will be interpreted as a high and anything less than the 1.5V limit is considered low. These settings are used on the outputs, so that input levels have flexible noise margins.

5.4.3 Characterization at Temperatures

Why characterize at different temperatures?

PLX devices are characterized at various temperature ranges to check for signal degradation. Signal timing will degrade with an increase in temperature; therefore, as devices are characterized at different temperatures the variation in timing (Δt) is monitored. If there is a significant change in timing due to temperature changes, then the fabrication or assembly process may become suspect. PLX characterizes devices at three different temperature ranges. The temperature levels are defined as follows:

Cold Temperature Test: 0°C, -40°C

Room Temperature Test: 25°C

Hot Temperature Test (worst case): 85°C

5.4.4 High Speed Digital Testers

High-speed digital testers are used specifically for production testing, device characterization and troubleshooting.

6. Failure Analysis

6.1 Failure Mechanisms

A physical or chemical process that causes a device to fail is termed the failure mechanism. Failure mechanisms can usually be placed into one of three categories, chip-related failures, assembly-related failures, and miscellaneous or application related failures. Some examples of chip related failures are metal line electromigration, diffusion-related failures, and oxide defects. Assembly related failures might be chip mounting, wire bonding, or packaging failures such as cracked or deformed device packaging.

6.2 Failure Probabilities

One device failure in 10^9 device-operating hours is defined as one Failure in Time (FIT). Failure rates, expressed in units of FITs, is traditionally defined as:

$$F(t) = [(Number\ of\ device\ failures) / (Number\ of\ operating\ devices \times Operating\ time)] \times 10^9$$

The failure rate $F(t)$ represents the instantaneous rate of device failure per device surviving at a time t . The FIT rates indicate the probability that a device will fail within a given amount of time during the so-called “useful life” of a device. The “useful life” of a device falls between the early stages of a products life (early failure period) and the time towards the end of a products life (wear out period). A graph of the hazard rate of a device gives rise to the popular “bathtub” curve, shown in Figure 6-1. FIT rates give a good indication to the operational reliability of our devices. To get lower FIT rates, the number of defects per a specified number of devices (typically measured in ppm or parts per million) must be reduced to as small a number as possible.

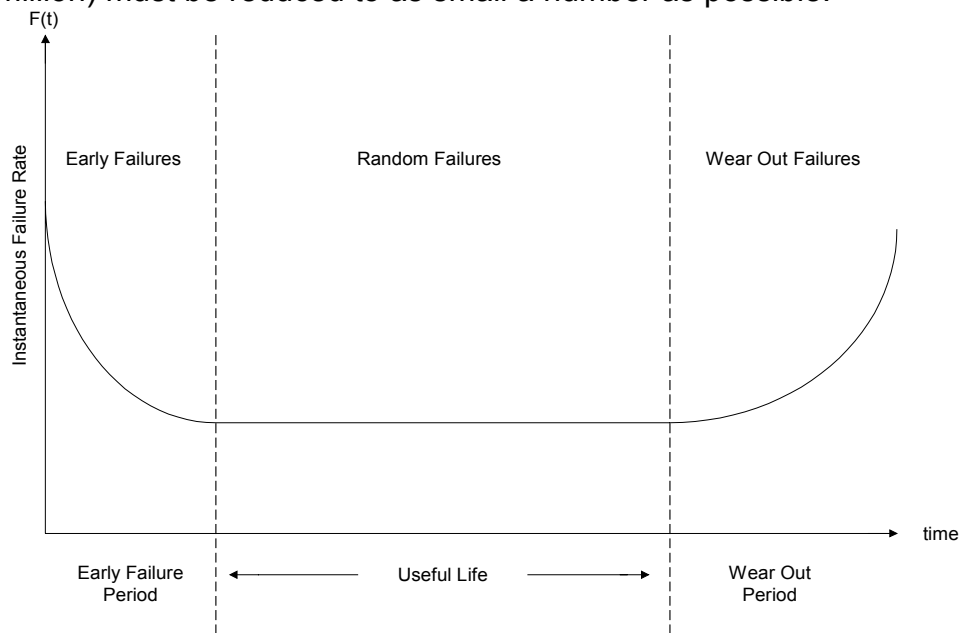


Figure 6-1. Failure Curve for Semiconductors

6.3 FIT Rates

Table 6-1. Calculated FIT Rate for Current PLX Products

Device	FIT Rate
PCI 9030	TBD
PCI 9050	30 FITS
PCI 9052	30 FITS
PCI 9054	< 87 FITS
PCI 9060 (series)	30 FITS
PCI 9080	30 FITS
IOP 480	40 FITS

7. General Product Information

This section provides general information specific for current production devices produced by PLX Technology.

7.1 Fabrication Process Technology

All current production PLX devices are Complementary Metal Oxide Semiconductor (CMOS) circuits. Table 7-1 gives a comparison of the process technology for any given PLX device. The process technology typically refers to the minimum feature size for a particular integrated circuit.

Table 7-1. Device Process Technology

PLX Device	Process Technology (μm)
PCI 9030	0.35
PCI 9050	0.60
PCI 9052	0.50
PCI 9054	0.35
PCI 9060-3A	0.60
PCI 9060ES	0.60
PCI 9060SD	0.60
PCI 9080-3	0.50
IOP 480	0.35

7.2 Device Packaging Terminology

There are various package types that are used for PLX products. These packages are:

PQFP – Plastic Quad Flat Package

PBGA – Plastic Ball Grid Array

LBGA – Low Profile Ball Grid Array

μ BGA – μ -Ball Grid Array (Micro-BGA)

7.3 Device Packaging Configurations

Table 7-2. Packaging Configuration

PLX Part number	Package Type	Lead/Ball Count	Packaging Dimensions (mm)	Lead/Ball Pitch (mm)
PCI9030-AA60PI	PQFP	176	26 x 26	0.5
PCI9030-AA60BI	μBGA	180	12 x 12	0.8
PCI9050-1	PQFP	160	31 x 31	0.65
PCI9052	PQFP	160	31 x 31	0.65
PCI9054-AA50PI	PQFP	176	26 x 26	0.5
PCI9054-AA50BI	PBGA	225	27 x 27	1.5
PCI9054-AB50PI	PQFP	176	26 x 26	0.5
PCI9054-AB50BI	PBGA	225	27 x 27	1.5
PCI9060 (series)	PQFP	208	31 x 31	0.5
PCI9080-3	PQFP	208	31 x 31	0.5
IOP480-AA66PI	PQFP	208	31 x 31	0.5
IOP480-AA66BI	PBGA	225	27 x 27	1.5

7.4 Device Packaging Diagrams

Figure 7-1 and Figure 7-2 show the relationship between a chip and/or die and encapsulate packaging for PQFP and PBGA packaging technologies respectively. The drawings are used for illustrative purposes only and are not to scale.

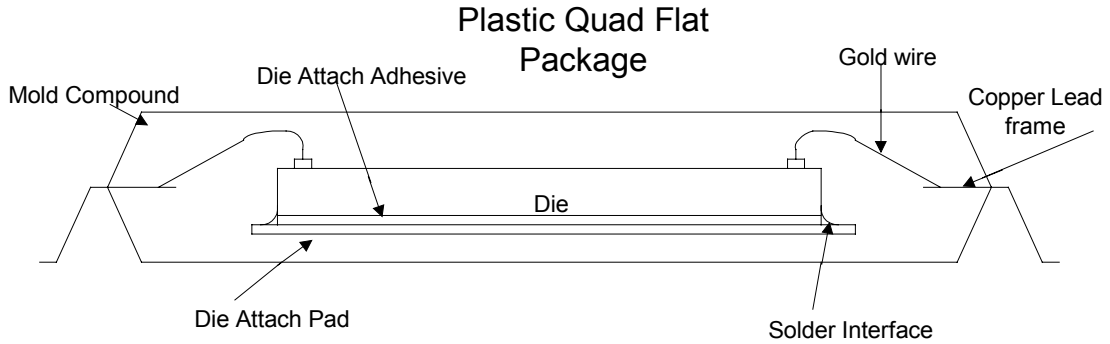


Figure 7-1. PQFP Packaging, Cross Sectional

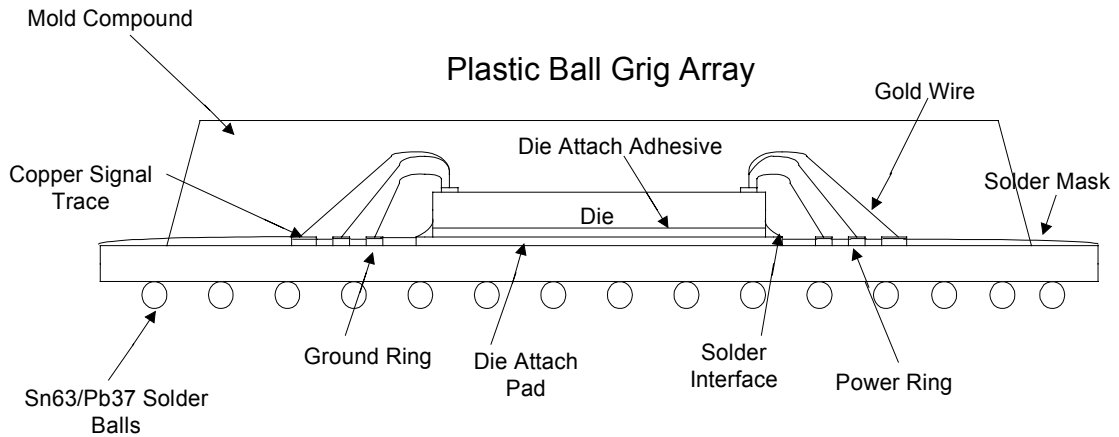


Figure 7-2. PBGA Packaging, Cross Sectional

7.5 Part Number Definitions

7.5.1.1 Current Part Number Labeling Method

¹ ² ³ ⁴ ⁵ ⁶
XXXX XXXX – XX XX X X

- 1) Device Class (i.e. **PCI**9054-AB50PI)
- 2) Part Number (i.e. PCI**9054**-AB50PI)
- 3) Device Revision I.D. (i.e. PCI9054-**AB**50PI)
 - AA, AB, AC, ...
- 4) Maximum Local Bus Operating Frequency (in MHz) (i.e. PCI9054-AB**50**PI)
- 5) Packaging Technology (i.e. PCI9054-AB**50**PI)
 - P = PQFP
 - B = PBGA or μ BGA
- 6) Operational Temperature Range (i.e. PCI9054-AB50**PI**)
 - I = Industrial (-40°C – 85°C)

7.5.1.2 Former Part Number Labeling Method

¹ ² ³
XXX XXXX – X

- 1) Device Class (i.e. **PCI**9080- 3)
- 2) Part Number (i.e. PCI**9080**- 3)
- 3) Revision Number (i.e. PCI9080- **3**)

7.6 PLX Device Class Types

PCI — PCI bus I/O Accelerator Bridge Device

IOP — Input/Output Processor

GBP — GigaBridge™ Port Switch Fabric Controller

7.7 Tray Types

All production-shipping trays used by PLX Technology are high temperature (150°C) bakable trays. Furthermore, all tray types adhere to JEDEC standards. The device count per tray depends on the device packaging configuration. The various part counts per tray can be broken down as illustrated in Table 7-3.

Table 7-3. Tray Loading

Package Type	Parts per Tray	Parts per Row	Parts per Column
160- pin PQFP	24	8	3
176- pin PQFP	36	9	4
208- pin PQFP	24	8	3
180- ball μ BGA	168	21	8
225- ball PBGA	40	10	4

8. References

Sung-Mo Kung, and Yusuf Leblebici. CMOS Digital Integrated Circuits: Analysis and Design. 2nd Ed. McGraw-Hill: San Francisco, 1999.

Glaser/Subak-Sharpe, Integrated Circuit Engineering. Addison-Wesley Publishing Co. Reading: Massachusetts, 1977.

JEDEC Solid State Technology Association, "Latch-up in CMOS Integrated Circuits" JEDEC Standard No.17, August 1998.

"High Temperature Storage Life", JESD22-A103-A, July 1989.

"Temperature Cycling", JESD22-A104-A, December 1989.

"Bias Life", JESD22-A108-A, March 1991.

"Highly Accelerated Temperature and Humidity Stress Test", JESD22-A110-B, February 1999.

Electronic Industries Association (EIA), JEDEC Solid State Technology Association. "Steady State Temperature Humidity Bias Life Test", EIA/JESD22-A101-B, April 1997.

"Solderability Test Method", EIA/JESD22-B102-C, September 1998.

IPC/JEDEC Standards, "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices", IPC/JEDEC J-STD-020-A, April 1999.

United States. Department of Defense. MIL- STD- 883, Military Standards Test Methods and Procedures for Microelectronics,

Solder Reflow Technology Handbook. Research International, Online, www.research-intl.com. Internet. 2000.

Perry, Guy. Basic Test Technology, Rev. 1.2, Soft Test, Inc., San Jose, 1994.

"How to Construct a Highly Accurate SPICE Model for the Signal Integrity Simulation of a High Speed Ball Grid Array Burn-In and Test Socket," 3M Company, Tech Paper, #80-6106-0858-2, 1994.

"Monitored Burn-in, An Overview," Micro Control Company, Test Application Series, Publication# 990046, 1980.

Appendix A. Definition of Terms

Input Pin: A device pin that acts as a buffer between the external signals and the internal logic.

Output Pin: A device pin that acts as a buffer between the internal logic and the external signals. The output pin provides IOL/IOH current.

Positive current flow: The current flowing from the external environment to the device.

Negative current flow: The current flowing from the device to the external environment.

Tri-State Output: A device output pin that has the capability of going into a high impedance state (high-Z state).

PMU: A precision measuring unit is capable of making accurate DC measurements by either forcing voltage and measuring current, or forcing current and measuring voltage.

DUT: The device under test.

VIL (Voltage input low): The voltage value applied to an input when applying a logic-0. VIL is the maximum voltage value that can be applied and still be recognized as a logic-0.

VIH (Voltage input high): The voltage value applied to an input when applying a logic-1. VIH is the minimum voltage value that can be applied and still be recognized as a logic-1.

VOL (Voltage output low): The voltage value produced by an output when driving a logic-0. VOL is the maximum value produced by the output when producing a logic-0.

VOH (Voltage output high): The voltage value produced by an output when driving a logic-1. VOH is the minimum value produced by the output when producing a logic-1.

IOL (Current output low): The amount of current that flows from the tester through the DUT output pins to ground, “sink current”, when the output is at a logic-0. The output must supply a specified amount of IOL current while maintaining the correct VOL voltage.

IOH (Current output high): The amount of current that must flow from the device pin to the test system, “source current”, while driving a logic-1. The output must supply a specified amount of IOH current while maintaining the correct VOH voltage.

IIL (Low input leakage current): The maximum current allowed to flow out of the input pin when a low voltage is forced onto the pin.

IIH (High input leakage current): The maximum current allowed to flow out of the input pin when a high voltage is forced onto the pin.

V_{DD} : The supply voltage for a MOS device.

I_{DD} : The supply current for a MOS device.