

PEX 8624 Highlights

- 24-lane, 6-port PCIe Gen 2 Switch
- Compliant to the PCIe base spec r2.0
- Integrated Non-Transparent port
- 2KB maximum payload size
- Microsoft Vista compliant
- *performancePAK™* features
- Full line rate on all ports
- Non-blocking switch fabric
- *visionPAK™* features
 - Serdes eye capture
 - Per port performance monitoring
 - Error injection and loopback
 - Packet Generator
- 180ns max packet latency (x8 to x8)
- Per port error diagnostics
- Advanced error reporting
- Port status bits and GPIO
- INTA# and FATAL_ERR# signals
- Memory (RAM) error correction
- Data path parity
- ECRC and Poison bit support
- 3 hot-plug ports with native hot-plug signals
- All ports hot-plug capable thru I²C

Application:

Server and Storage Systems

PLX Product:

PEX 8624 – 24-lane, 6-port PCIe Gen 2 Switch

Key Benefit:

PCIe Fan-Out for SSD Apps

Building SSD with PCIe Gen 2

Recent developments in FLASH memory technology have made it possible for system designers to build large banks of non-volatile memories without sacrificing the robustness and reliability of the system. Solid State Drives (SSD) are common in many advanced or boutique systems. With the latest reduction in prices, increase in endurance, and better error correction, MLC FLASH is being considered for designs in enterprise systems and high-end consumer devices.

Traditional, SSDs consist of a SATA interface, a SATA to FLASH controller, and array of FLASH devices (as shown below). This is about to change as more vendors adopt PCIe in their FLASH controllers.

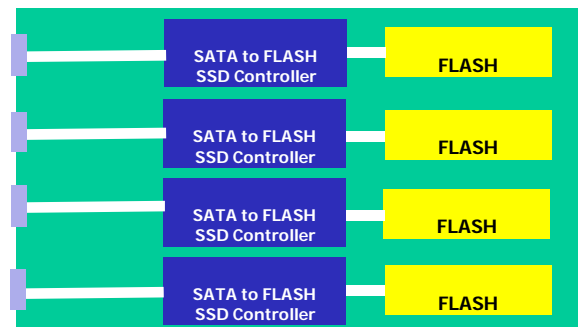


Figure 1. SATA Based Solution

New state-of-the-art systems are using PCIe 2.0 to take advantage of the bandwidth offered in PCIe 2.0 based chipsets and processors. Currently, most RISC CPUs and all new server/storage chipsets for x86 CPUs offer PCIe Gen 2 interfaces. The industry is moving towards the standards like non-volatile memory host controller interface (NVMHCI) that use PCIe switches as the aggregation point for SSDs.

PLX PCIe Gen 2 switches are perfect for these applications with a broad variety of switches that can service any possible need for aggregation and switching. PCIe Gen 2 offers 5GT/s line rate per lane, which can be scaled to x2, x4, x8 and x16. PLX's PEX

8624 offers six x4 PCIe Gen 2 ports. In SSD applications, a common use of PEX 8624 is to connect a x8 port to the host and four x4 ports to the FLASH controllers - thus aggregating four arrays of FLASH memories to the host.

PEX 8624 – 6 ports & debug features

This document focuses on PEX 8624 but most of the features, capabilities and benefits discussed here also apply to other PLX PCIe Gen 2 switches.

SATA Based Solution:

Most SSDs sold today use SATA interfaces and in some applications several SATA FLASH controllers are aggregated though SATA port multipliers that connect to the host through a PCIe interface as shown in Figure 2.

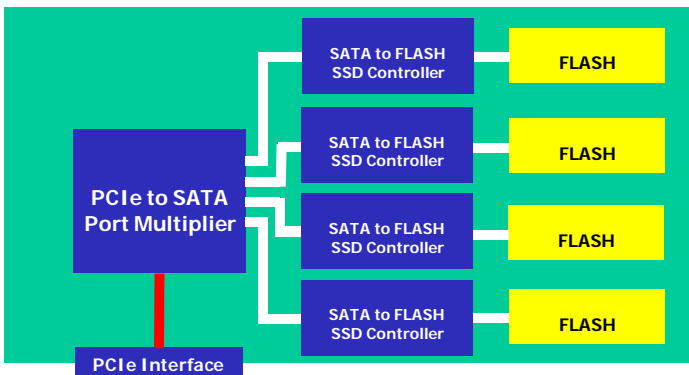


Figure 2. SATA Based Solution

PCIe Based SSD Add-in Card:

Most FLASH controller vendors are either developing or shipping products with a PCIe interface to take advantage of ubiquity, scalability and new standards. Some are even removing the SATA protocol stack in software to reduce the overhead associated with it.

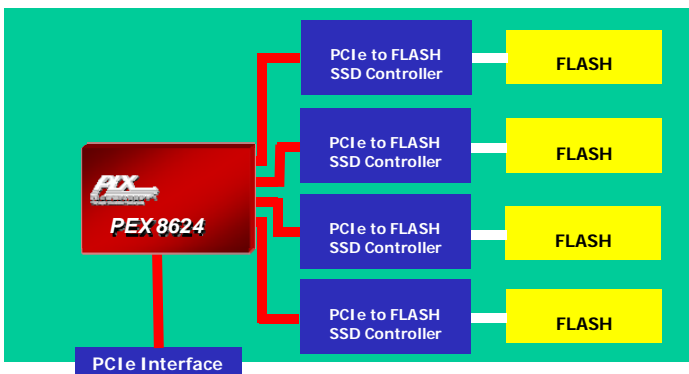


Figure 3. PEX 8624 Based SSD Add-in Card

PCIe Based Large SSD Bank:

New enterprise applications are hungry for large arrays of FLASH memory for data mining, transaction processing,

searching, etc. Large port and lane count switches such as PEX 8696 are available from PLX to aggregate larger numbers of SSD arrays. In this design, the PEX 8696 host port can be bifurcated (or split in multiple ports) to connect to multiple hosts to offer host redundancy or sharing of the FLASH arrays amongst multiple hosts.

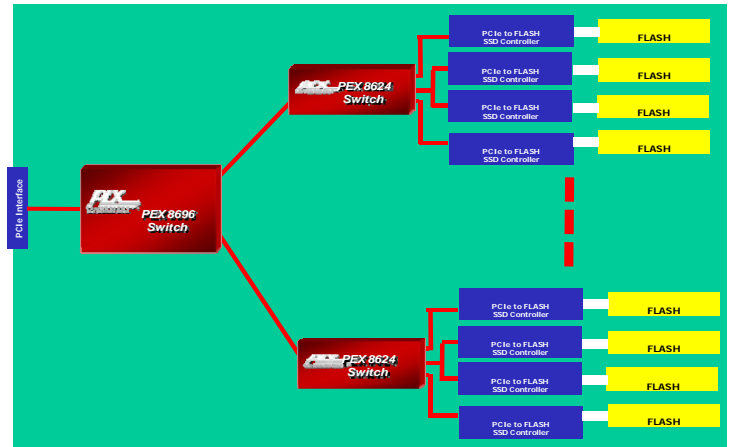


Figure 4. Large SSD Array Aggregation

PLX offers best-in-class debug tools:

The *visionPAK* toolset of any PLX PCIe Gen 2 switch is a combination of features designed and integrated in the silicon and software developed to allow ease of use. *visionPAK*, through a user friendly interface, enables the following:

- Access and measurement of RX eye on internal pads
- Error injection in the data path to see system behaviors
- Packet generation to saturate up to x16 wide Gen 2 port
- Monitor errors, link utilization and performance
- PRBS and loop-back at various stages of data path
- Access to internal parallel data path and state-machines
- View of the PCIe hierarchy of the system

Additional PLX Advantages

In addition to the above key features PLX switches support Non-transparent bridging for host isolation, dynamic buffer/credit allocation for enhanced performance and advanced power management techniques.

Additionally, the following features are also supported:

- Any port can be programmed as the upstream port
- Read Pacing™ for fair bandwidth allocation
- Advanced error reporting
- Per port error diagnostics

Available on PLX Website:

Product Brief, Databook, Application Notes, technical support <http://www.plxtech.com/8624>