

PEX 8604 Highlights

- **PEX 8604 Vitals**
 - 4-lane, 4-port PCIe Gen 2 switch
 - Integrated 5.0 GT/s SerDes
 - 15 x 15mm², 196-ball PBGA package
 - Typical Power: 1.29 Watts

- **PEX 8604 Key Features**
 - **Standards Compliant**
 - PCI Express Base Specification, r2.0 (backwards compatible w/ PCIe r1.0a/1.1)
 - PCI Power Management Spec, r1.2
 - Microsoft Vista Compliant
 - Supports Access Control Services
 - Dynamic link-width control
 - Dynamic SerDes speed control
 - **High Performance**
 - ◆ **performancePAK**
 - ✓ Read Pacing (bandwidth throttling)
 - ✓ Dynamic Buffer/FC Credit Pool
 - Non-blocking switch fabric
 - Full line rate on all ports
 - Packet Cut-Thru w/ 190ns max packet latency (x1 to x1)
 - **Flexible Configuration**
 - Ports configurable as x1, x2
 - Registers configurable with strapping pins, EEPROM, I²C, or host software
 - Lane and polarity reversal
 - Compatible with PCIe 1.0a PM
 - **Multi-Host & Fail-Over Support**
 - Configurable Non-Transparent (NT) port
 - Failover with NT port
 - **Quality of Service (QoS)**
 - Eight traffic classes per port
 - Two Virtual Channels (VCs)
 - Weighted round-robin source port arbitration
 - **Reliability, Availability, Serviceability**
 - ◆ **visionPAK**
 - ✓ Per Port Performance Monitoring
 - Per port payload & header counters
 - ✓ SerDes Eye Capture
 - ✓ Error Injection and Loopback
 - All ports Hot-Plug capable thru I²C (Hot-Plug Controller on every port)
 - ECRC and Poison bit support
 - Data Path parity
 - Memory (RAM) Error Correction
 - INTA# and FATAL_ERR# signals
 - Advanced Error Reporting
 - Port Status bits and GPIO available
 - Per port error diagnostics
 - JTAG AC/DC boundary scan

Application: **Bandwidth Bridge**

PLX Products:
PEX8604 – 4-lane, 4-port PCIe Gen 2 Switch
PEX8608 – 8-lane, 8-port PCIe Gen 2 Switch

Key Benefit:
Gen 2 speeds; Low power; small package; Fan-Out

Bandwidth Bridge

For several years now, PCI has been a key interconnect in embedded CPUs and SoCs that are used in consumer applications. Recently, these embedded CPUs and SoCs have migrated the IO interface from a parallel PCI bus to a serial PCIe implementation. Because PCIe is a high-speed serial interconnect, it is not uncommon to see a PCIe interface (at PCIe Gen1 speed of 2.5 Gbps) with either a 1 x2 or 1 x4 being implemented. A number of such DSPs and CPUs from vendors like LSI, Freescale, TI, AMCC, Cavium and Netlogic are now available with these 1 x4 or 1 x2 Gen1 (or 2 x1 Gen1 which can be combined into 1 x2 Gen1) interfaces. However, these components need to connect to endpoints such as USB3.0 or SATA6. Due to the mismatch in bandwidth, customers need a switch that can support both PCIe Gen1 and Gen2 speeds independently.

Bandwidth Bridge Using PEX8608

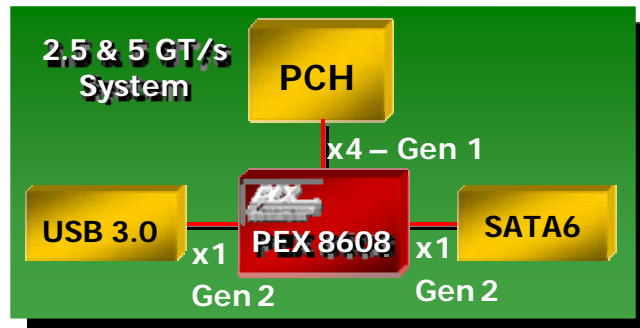


Figure 1. PEX8608 as a Bandwidth Bridge

In Figure 1, the upstream port on PEX8608 is providing a connection to the Platform Controller Hub from Intel via a 1 x4 Gen 1 PCI Express interface for a total throughput of 4 x 2.5 Gbps = 10 Gbps. The downstream ports of PEX8608 are connected to USB 3.0 via a PCI Express Gen 2 (5 Gbps) interface and also SATA6 via a PCI Express Gen 2 (5 Gbps) interface. So the total bandwidth in the downstream direction on PEX8608 is 10 Gbps (5 Gbps to the USB 3.0 interface and 5 Gbps to the SATA 6.0 interface). This is a load-balanced system with 10 Gbps in either direction. This is made possible because of the PLX PEX8608 switch.

Figure 2 shows an example of how PEX8604 can be used to achieve the same functionality, at a lower cost.

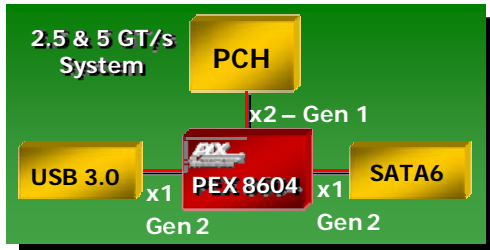


Figure 2. PEX8604 as a Bandwidth Bridge

In Figure 2 the upstream port on PEX8604 is providing a connection to the Platform Controller Hub from Intel via a 1 x2 Gen 1 PCI Express interface for a total throughput of $2 \times 2.5 \text{ Gbps} = 5 \text{ Gbps}$. The downstream ports of PEX8604 are connected to USB 3.0 via a PCI Express Gen 2 (5 Gbps) interface and also SATA6 via a PCI Express Gen 2 (5 Gbps) interface. So the total bandwidth in the downstream direction on PEX8608 is 10 Gbps (5 Gbps to the USB 3.0 interface and 5 Gbps to the SATA 6.0 interface). In this example, obviously the upstream is only 5 Gbps but the downstream is 10 Gbps – causing a mismatch. However this usage model assumes that the upstream port on PEX8604 is not saturated completely – this usage model has the added benefit of a lower-cost PEX8604, compared to PEX8608.

Increasing the connectivity

As can be observed from both Figure 1 and Figure 2, the PEX8604 and PEX8608 devices, in addition to acting as a bandwidth bridge between Gen 1 and Gen 2 speeds, increase connectivity for the PCH by offering fan-out connection to the PCH.

The PEX8604 consists of four lanes and four ports each with x1 link widths and 5.0 GT/s SerDes (also can work at 2.5Gbps).

Config	Port 0	Port 1	Port 2	Port 3
0 Default	x1	x1	x1	x1
1	x2	x1	x1	
2	x2	x2		

Figure 3. PEX8604 Configurations

The PEX8608 consists of eight lanes and eight ports each with x1 link widths and 5.0 GT/s SerDes (also can work at 2.5Gbps).

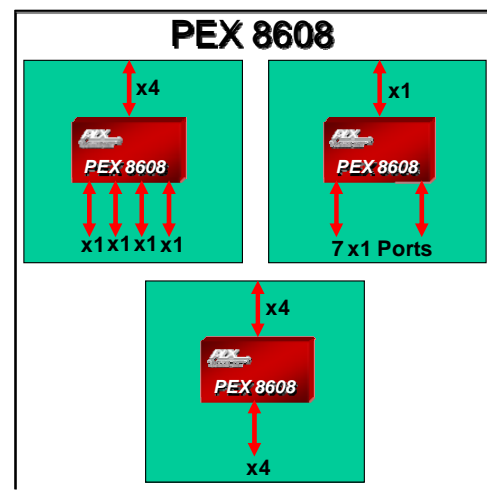


Figure 4. PEX8608 Configurations

Additional PLX Advantages

- *visionPAK*
 - SerDes Eye Width Capture
 - Per Port Performance Monitoring
 - Error Injection & Loopback
- Integrated Non-Transparent Port
- Spread Spectrum Clock Isolation

Available on PLX Website:

www.plxtech.com/8604; www.plxtech.com/8608

Product Brief, Databook, Application Notes, Technical Support Hardware (RDK) and Software (SDK) Development Kits, Signal Integrity (SI) Kit, BSDL models, H-Spice models, OrCAD symbols