

PEX 8696 Highlights

- **PEX 8696 Vitals**
 - 96-lane, 24-port PCIe Gen 2 switch
 - Integrated 5.0 GT/s SerDes
 - 35 x 35mm², 1156-ball FCBGA package
 - Typical Power: 10.2 Watts

- **PEX 8696 Key Features**
 - **Standards Compliant**
 - PCI Express Base Specification, r2.0 (backwards compatible w/ PCIe r1.0a/1.1)
 - PCI Power Management Spec, r1.2
 - Microsoft Vista Compliant
 - Supports Access Control Services
 - Dynamic link-width control
 - Dynamic SerDes speed control
 - **High Performance**
 - ◆ **performancePAK**
 - ✓ Read Pacing (bandwidth throttling)
 - ✓ Multicast
 - ✓ Dynamic Buffer/FC Credit Pool
 - Non-blocking switch fabric
 - Full line rate on all ports
 - Packet Cut-Thru w/ 176ns max packet latency (x16 to x16)
 - 2KB Max Payload Size
 - **Flexible Configuration**
 - Ports configurable as x1, x2, x4, x8, x16
 - Registers configurable with strapping pins, EEPROM, I²C, or host software
 - Lane and polarity reversal
 - Compatible with PCIe 1.0a PM
 - **Multi-Host & Fail-Over Support**
 - Configurable Non-Transparent (NT) port
 - Failover with NT port
 - Up to Eight upstream/Host ports with 1+1 or N+1 failover to other upstream ports
 - **Quality of Service (QoS)**
 - Eight traffic classes per port
 - Weighted round-robin source port arbitration
 - **Reliability, Availability, Serviceability**
 - ◆ **visionPAK**
 - ✓ Per Port Performance Monitoring
 - Per port payload & header counters
 - ✓ SerDes Eye Capture
 - ✓ Error Injection and Loopback
 - 4 Hot-Plug Ports with native HP Signals
 - All ports hot-plug capable thru I²C (Hot-Plug Controller on every port)
 - ECRC and Poison bit support
 - Data Path parity
 - Memory (RAM) Error Correction
 - INTA# and FATAL_ERR# signals
 - Advanced Error Reporting
 - Port Status bits and GPIO available
 - Per port error diagnostics
 - JTAG AC/DC boundary scan

Application:

Fan-Out in Systems Using the Jasper Forest CPU

PLX Products:

PEX8696 – 96-lane, 24-port PCIe Gen 2 Switch

PEX 8624 – 24-lane, 6-port PCIe Gen 2 Switch

Key Benefit:

High Lane/Port Count Fan-Out

Jasper Forest

Intel recently announced Jasper Forest, their latest CPU. The Jasper Forest CPU will be available in early 2010 and will target the embedded, communication, and storage markets. Jasper Forest will offer 16 Gen 2 PCI Express (PCIe) lanes and one Non-Transparent (NT) port. This NT port will be configurable as either a x4 or x8 port and will support PCI's Non-Transparent Bridging functionality for host isolation. In a PCIe hierarchy, there can only be one host for each endpoint. For multi-host architectures with multiple CPUs, a NT port is needed to isolate the host hierarchies and ensure there is no contention over the endpoints.

The NT port allows systems to isolate host memory domains by presenting the processor subsystem as an endpoint rather than another memory system. Base address registers are used to translate addresses; doorbell registers are used to send interrupts between the address domains; and scratchpad registers (accessible by both CPUs) allow inter-processor communication. Until now, the NT functionality was only available via a PCIe Switch. PLX Technology is the only switch vendor today offering Gen 2 switches with an integrated NT port. In fact, all of PLX's Gen 2 (PEX 86xx) Switches offer an NT port (configurable as x1, x2, x4, x8, or x16).

Although Jasper Forest offers an integrated NT port, the need for a PCIe switch will still remain. Jasper Forest's 16 lanes can be grouped into four (x4x4x4x4), three (x8x4x4), or two (x8x8) ports. In many applications this is already an insufficient amount of PCIe lanes and ports. Moreover, if one of these ports is used as an NT port, the need for more lanes – and therefore a switch – is intensified.

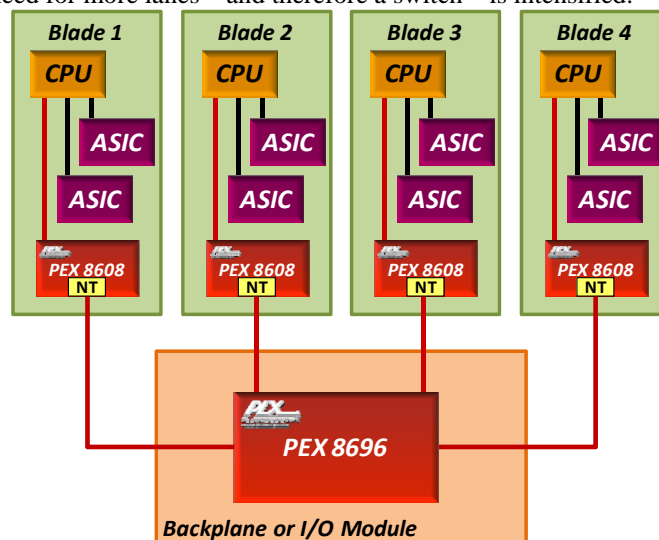


Figure 1

The Evolution of the CPU

In a traditional PCIe backplane usage model, one large PCIe switch (see PEX 8696 in Figure 1) is used on the switch fabric to fan-out to all of the processor and I/O blades. Since the processor blades have CPUs on-board, a smaller PCIe switch with an NT port is used to isolate the CPU domain on each processor blade. The PEX 8608 is typically used as a simply NT buffer, utilizing a x4 link on both the upstream and downstream sides of the switch.

In the past, the CPU would connect to a Northbridge (not shown) which would connect to the memory and graphics display port. Furthermore, the Southbridge (also not shown) would serve as the I/O hub providing all the necessary I/O ports. Hence, providing a large number of PCIe ports was not required by CPUs.

But going forward, the Northbridge has disappeared and the Southbridge only offers a limited number of PCIe lanes. As a result, the burden of providing the necessary PCIe ports to connect to memory, graphics, and I/Os falls on the CPU.

Moreover, the need for I/Os on a system only continues to grow. As designers try to differentiate their products and create specialized systems targeting niche market segments (e.g. high-end storage, super-computing, etc.), today's systems are often pumped full of endpoints and support numerous interfaces.

As a result, even though Jasper Forest's integrated NT port will eliminate some of the need for switches that provide host isolation, it will also create a need for additional PCIe ports. Using one of Jasper Forest's four PCIe ports (or two PCIe ports if using x8 links) as an NT port does not leave enough lanes on the Jasper Forest CPU to fan out to other endpoints such as memory, ASICs, or other I/O (SATA, NIC, HBA, etc.).

Figure 2 shows an example where a second switch (the PEX 8624) is used to fan out from the Jasper Forest CPU to its endpoints. In this example, one of Jasper Forest's ports is being

used as an NT port (could be x8 or x4) and the other PCIe port is used as a x8 link to the PCIe switch. The switch then fans out to four endpoints via x4 links (could be a mix of x8s and x4s as well). The PEX 8624 provides up to 24 lanes and 6 ports. A larger (e.g. PEX 8632) or smaller (e.g. PEX 8616) switch can also be used depending on how many I/Os need to be connected to the CPU.

In the backplane (or I/O module), the PEX 8696 is still used for fan-out purposes to provide a connection between all the CPU blades. Supporting up to 96 lanes and 24 ports, the PEX 8696 can support a large number of I/Os (capable of fanning out to 24 blades/modules via x4 links) and is ideal for fan-out applications.

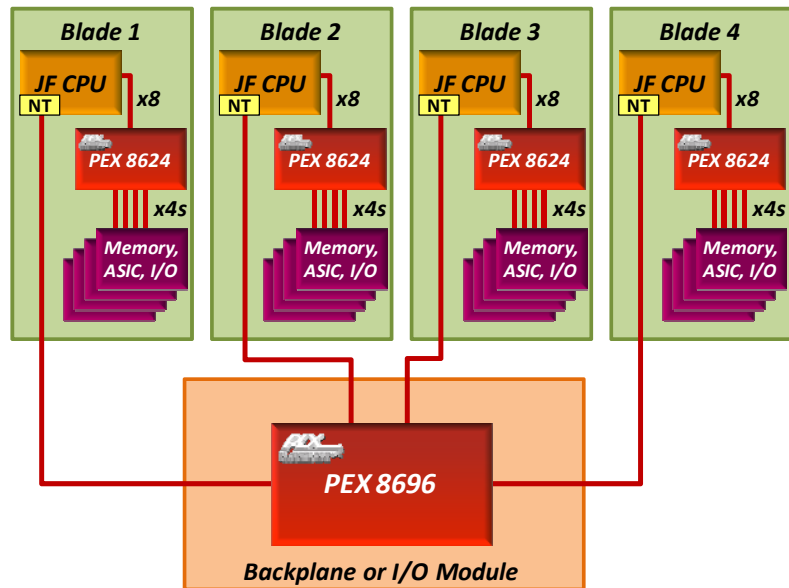


Figure 2

Additional PLX Advantages

Since the Jasper Forest CPU's integrated NT port can only support a max link-width of x8, applications requiring a x16 NT link will still require a PCIe switch. Furthermore, all of PLX's PCIe Gen 2 Switches are loaded with features targeted at enhancing overall system performance as well as debug capabilities. These features are part of PLX's *performancePAK* and *visionPAK* as listed below:

performancePAK

- Multicast
- Dynamic buffer/FC credit pool
- Read Pacing

visionPAK

- SerDes Eye Width Capture
- Per Port Performance Monitoring
- Error Injection & Loopback

Available on PLX Website:

www.plxtech.com/8696 and www.plxtech.com/8624

- Product Brief, Databook, Application Notes, Technical Support