

## PCI 9060ES Frequently Asked Questions

The PCI 9060ES FAQ details the most frequently asked questions about this PCI product. The information is divided into five categories: Direct Slave Access, Direct Master Access, DMA, Configuration Cycles, and Miscellaneous to reflect the major functionality of the device. The information in the FAQ will be continuously updated.

### Direct Slave Access

**1. Can the PCI 9060ES perform long burst?**

The PCI 9060ES can be programmed to perform single cycle, burst 4 (burst 4 Lwords at a time), and burst forever. When the burst mode is disabled in the Local Bus Region Descriptor Register, the PCI 9060ES performs single cycle. When burst mode is enabled and BTERM# input is disabled, it bursts up to 4 Lwords, i.e., bursting can start on any boundary and continue up to an address boundary. After the data at the boundary has been transferred, the PCI 9060ES generates a new address cycle (ADS#). When burst mode and BTERM# input are enabled, the PCI 9060ES performs long bursts. The PCI 9060ES will generate a new address cycle once BTERM# is asserted.

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**2. How can the wait state be generated on the local side of the PCI 9060ES?**

There are two ways to generate wait states. One way is to program the internal wait states in the "Local Bus Region Descriptor" register [LOC 98h] bit [5:2]. The other way is to enable the READYi# mode (again in the "Local Bus Region Descriptor" register and assert READYi# when the local side is ready to receive or provide data.

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**3. My Local Bus is exclusively 16 bit wide. The PCI bus is 32 bits wide. What do I need to do to communicate between the two buses?**

16-bit devices on the local bus is no problem. The PCI 9060ES can set Space 0 or the Expansion ROM to 16 or even 8 bits wide. It will simply break up the 32-bit accesses from the PCI side into multiple 16-bit transactions. A 16-bit processor will be using the 9060's SX mode for multiplexed 16-bit buses. External FIFO on the 16-bit bus present a slight problem as the PCI 9060ES always attempts to build 32-bit Lwords on direct slave reads. However, when prefetch is disabled and the PCI 9060ES prefetch is programmed for single reads, it will perform only a single 16-bit read regardless of the C/BE's on the PCI side.

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**4. I have multiple devices on my Local Bus but only one Direct Slave address space. How do I accomplish the Address mapping?**

A single address space can encompass several devices simply by

using address decoding to generate different chip selects on the local bus. If needed, the Expansion ROM space and Space 1 (SD only) can also be used. Changing bus sizing on the fly will be required if different bus sizes are used by different devices in the same address space.

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**5. When does the local bus latency counter start counting?**

The local bus latency counter starts after PCI 9060 first asserts ADS# on the local bus.

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**6. During the Direct Slave Accesses, do I need to read the addresses on every access or data phase?**

No. It is not necessary to read the addresses on every access or data phase. The integrated address counter in the PCI 9060ES increments the address automatically. The PCI 9060ES latches data on every rising edge of the local clock (LCLK) and holds it until READY# is received. However, an external address counter is needed in case of reading/writing to the local SRAM (Memory).

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### Direct Master Access

**1. Is it possible to perform Direct Master and Direct Slave transfers simultaneously?**

The PCI 9060 can handle Direct Master, Direct Slave, and DMA cycles all at the same time. Once the originator initiates the transfer, the PCI 9060 will handle all the arbitration. However, a simultaneous Direct Slave and Direct Master cycle can result in a deadlock. In this case, the PCI 9060 will request that one of the originators back off the bus.

### Configuration Cycles

**1. I am trying to configure another PCI device with the PCI 9060ES, but my system hangs when I try this. What could be causing the system hang during the to configuration accesses?**

Most likely you've hit on an IDSEL line with no device attached. Therefore, no DEVSEL is returned to the PCI 9060ES. This is defined as a PCI Master Abort. To recover from a Master Abort, a flag must be cleared from the PCI 9060ES's internal registers. Otherwise, no further Direct Master transactions can take place. The same applies to Target Abort situations.

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**2. Is the EEPROM programmable in the circuit?**

Yes. The EEPROM is programmable in the circuit through the EEPROM Control register (PCI 6Ch, LOC ECh). Bit 24 needs to be toggled to generate an EEPROM clock for every bit to be read/written to the EEPROM. A pre-programmed EEPROM (non-blank) is required for the system to boot properly. However

in the PCI9080, A blank EEPROM is supported. When a value of "FFFFFFFFh" is detected in the first word location, the PCI9080 loads its default values. The EEPROM can then be programmed by writing to the EEPROM Control register.

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**3. The PCI 9060ES does not seem to read the new EEPROM I've written, what can cause that?**

There are two possibilities: 1. PCI 9060ES supports "93CS46" EEPROM only. It does not support "93C46" EEPROM. 2. PE signal (pin #6 of the EEPROM) must be pulled-up through a 4.7K ohm resistor and PRE signal (pin #7) must be pulled-down through a 100 ohm resistor, respectively.

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**4. Do I program locations 00h and 01h to 055h and 0Aah, respectively, when I want to use a new EEPROM containing configuration information only?**

No. When using a new EEPROM containing configuration information only, locations 00h and 01h do not need to be programmed to 055h and 0AAH, respectively. That is only necessary when invoking the Expansion ROM.

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**5. How can I find the memory location of the add-in after the system boots up?**

PCI configuration register 18h contains the base address for Local Address Space 0 and Local configuration register 04h contains the local remap address. Therefore a configuration read access to PCI register 18h and Memory or I/O access to Local Configuration register 04h will indicate the memory location of the add-in card.

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**6. How long does it take to initialize the PCI 9060ES?**

If an EEPROM is connected to the PCI 9060ES then it takes anywhere from 172 (1 MHz EEPROM) clocks to 556 clocks to initialize the PCI 9060ES. If the EEPROM is not installed then the default value will be used. In this case it takes 12 (1 MHz EPROM) clocks. The PCI 9060ES detects the EEPROM present by reading a "0" at the start bit 0. If the EEPROM is detected, the information in the EEPROM will be loaded. If it is not detected, the PCI 9060ES's default value will be loaded. The PCI 9060ES supports "Short Load" by pulling down on SHORT# pin and "Long Load" by pulling SHORT# pin high. Five 32-bit words are stored sequentially in the EEPROM in "Short EEPROM Load" and seventeen 32-bit words are stored in "Long EEPROM Load". The EEPROM clock can be derived from the PCI clock or by using a 1MHz external oscillator.

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## Miscellaneous

**1. Does the Interrupt Control/Status register get reset when**

**issuing a "software reset"?**

No. The "software reset" only resets the local configuration registers and not the PCI configuration registers or Shared Runtime registers.

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**2. Is it possible to write to the Expansion ROM Space? What if my BIOS boots an enabled Expansion ROM as code?**

The Expansion ROM space is simply a memory window for Direct Slave transactions. There is no restriction on reads or writes as long as the PCI 9060ES is configured to point to a writable device. Changing the access code will insure that the Expansion ROM contents are not run during boot up as code by BIOS. Another solution is to disable the Expansion ROM space at startup and later to enable it. But by then, BIOS may have already allocated all available PCI spaces. A workaround is to map Space 0 bigger than necessary during boot up, then afterwards, reducing its size and enabling the expansion ROM space at that time. The Expansion ROM space can then be mapped to the area that Space 0 just vacated.

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**3. Does PLX provide a Verilog Model for the PCI 9060ES?**

Yes. PLX provides models for all of our 9060 family of product through a third party vendor. This model can be acquired from Simutech, Inc.

*19545 NW vonNeumann Dr. Suite 135  
Beaverton, Oregon 97006  
<http://www.simutech.com>*

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**1. Is the PCI 9060ES PCI 2.1 compliant?**

The PCI 9060ES is PCI 2.1 compliant. In particular, it supports "Delayed Read Transaction", i.e., when the PCI master performs a "Direct Slave Read" access to the local bus, the PCI 9060ES immediately issues a retry to the PCI bus. In the mean time, it requests the read data from the local bus and queues it in the FIFO. So when the PCI master returns to fetch read data again, the read data is now ready. The "Delayed Read Transaction" function is programmable through the 9060ES's configuration register.

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**2. How can I acquire the source code for the software files listed on the PLX web site?**

Contact your local PLX representative or send the request to [apps@plxtech.com](mailto:apps@plxtech.com).

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**3. How much logic do I need to make my add-on state machine?**

PCI 9060ES provides a glueless interface to the i960. It also supports other processors: Motorola 68040, PowerPC 403, and 603 are just some, with some glue logic. Please refer to the PCI Bus Interface and Clock Distribution Application Notes for more detailed information on Schematic Orcad files, PAL equations, etc., for interface between PCI 9060ES and other microprocessors.

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**4. How much power does the PCI 9060ES use and what is it's thermal characteristics?**

The maximum power supply current ( $I_{cc}$ ) for the PCI 9060ES is 120mA. This power consumption is measured at  $V_{dd}$  equals 5.25V and PCI/Local clock equal 33Mhz.

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**5. Are any pull up or pull down resistors required for the PCI 9060ES?**

For Add-in cards, PCI bus interface signals do not require any pull up or pull down since they are already handled by central resources on the motherboard or the backplane. For embedded systems, however, pull-ups are needed for PCI bus interface signals. All Local bus interface input signals contain internal pull-up through a 10K ohm resistor, and therefore a pull-down resistor is needed for any active high signal. External pull-up/pull-down resistors are required for Local input/output signals. For good design practice all input and input/output signals should be pull-up/pull-down to an in-active state when they are not driven by anybody.

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**6. Is it possible to detect which revision level the PCI 9060ES is?**

Yes. The revision ID is located in the PCI Revision Register (Offset 08h). This register is readable from both PCI and Local side.

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**7. How do I initiate a FIFO transfer?**

The FIFO transfer is initiated automatically. Data transfers from PCI-to-Local or Local-to-PCI during Direct Slave Accesses, Direct Master Accesses and DMA operation must go through the internal FIFO. The PCI 9060ES manages all aspects of the FIFO on transfers initiated as a read or write.

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**8. How is the FIFO advance determined?**

PCI 9060ES contains integrated address counter. Local address is incremented automatically on the rising edge of the local clock unless wait state is added.

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**9. How do I perform Endian conversion?**

Endian conversion can be performed through software (programming local configuration register) or controlled by hardware (BIGEND# input pin).

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**10. How can I generate an interrupt to the PCI bus from the add on side?**

There are two ways to generate an interrupt to the PCI bus from the add on side: Write to the Local-to-PCI doorbell register and set a 1 to bit [8] and bit [9] of the Interrupt Control/Status register (LOC E8h). Assert LINTi# to the PCI 9060ES and set a 1 to bit [8] and bit [11] of the Interrupt Control/Status register (LOC E8h).

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